LINE SKIP COMMUTATOR FOR A SOLID STATE CELESTIAL FIELD SCANNER

W. H. HELL, J. M. HANLET, R. W. HAAS

FEBRUARY 1969

CONTRACT NO. NAS 12-521

Prepared By

THE MARQUARDT CORPORATION

16555 Saticoy Street
Van Nuys, California

For

NATIONAL AERONAUTICS AND SPACE ADMINISTATION

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SUMMARY

The objective of this contract was to demonstrate the feasibility of fabricating a line skip commutator in a thin film configuration suitable as a readout device for the Marquardt Ferrotron image sensor plate in celestial field scanner applications. A logic study provided a configuration that permits readout by line skip commutation rather than sequential scanning of an image plate and eliminates the possibility of ambiguity in a matrix readout. A hybrid thin film configuration of the commutator was fabricated and tested thus confirming feasibility of operation. A development program in the use of ion implantation techniques for the fabrication of active thin film switching elements was initiated.

INTRODUCTION

This report describes the work performed under Contract NAS 12-521 for the period March, 1967 to September, 1968. The primary objective was to investigate the feasibility of implementing a line skip commutator in thin film configuration as a readout mechanism for the Marquardt Ferrotron image sensor plate in celestial field scanner applications. The immediate goal was to establish the basic commutator logic configuration, to experimentally demonstrate the feasibility of line skip readout employing hybrid thin film circuits in conjunction with a simulated image plate and to investigate advanced fabrication techniques for a high resolution implementation.

In a celestial field scanner, a selected stellar field is imaged upon a photosensitive surface, which, in turn, is electronically read out element by element to determine the relative positions of stars or other celestial objects. For the purpose of space-borne applications, it is desirable to use for the sensing and readout functions solid state, thin film components which require minimum weight and power, and offer maximum reliability. In principle, the Marquardt image sensor is a plate where a matrix of photosensitive/storage elements combined with a readout commutator are deposited by thin film techniques onto a common substrate.

For high quality star field image transducing it is necessary to scan a very large number of image points within a given field of view. Since only a very few image points are illuminated by radiating sources in that field, a conventional raster mode of readout yields a very low data rate. The data rate can be considerably increased when employing a line skip mode of readout which scans only those elements that contain data, i.e., it sequentially identifies only the location of the data points.

To implement the subject program it was first necessary to analytically investigate the sensor/commutator interface aspects in conjunction with the functions to be performed in the line skip operation. This study culminated in the delineation of the logic circuit and the determination of performance characteristics of the pertinent thin film components.

As a next step, the feasibility of producing the logic switching elements from a material that is compatible with that employed in the sensor was investigated in conjunction with another program. A common material for commutator and sensor is desirable when depositing commutator and sensor onto the same substrate.

Ultimately, the line skip commutator is to operate in conjunction with a high resolution image plate. The large number and very small size of the switching elements that have to be integrated with each image plate matrix readout line requires a special fabrication technique. A theoretical and experimental investigation was initiated on the use of ion plating technique which would allow the necessary high packing density of switching elements.

In order to demonstrate the feasibility of non-ambiguous line skip readout in two axis, a breadboard model was prepared employing hybrid thin film techniques.

CONCEPT

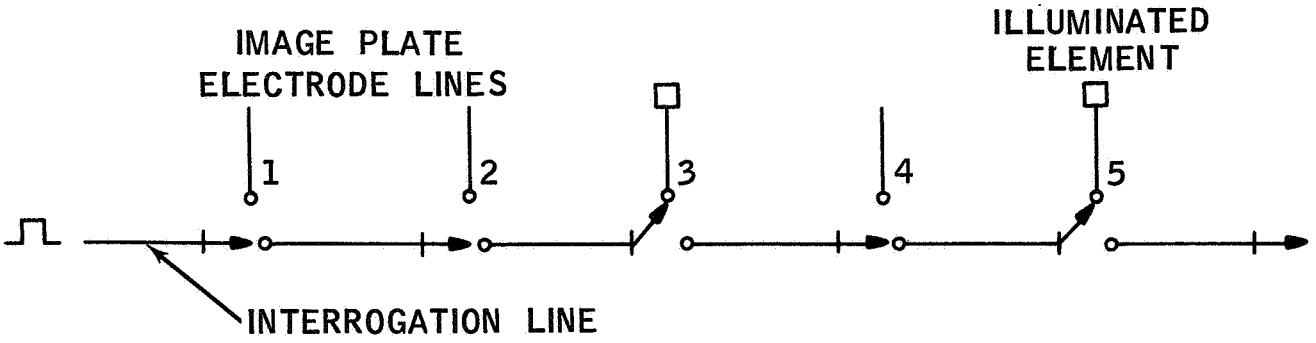
The Ferrotron image plate is composed of a photoconductor and a ferroelectric material laminate. During exposure to a scene the incident light controls the current flowing through the photoconductor as a function of its intensity at any given image point and the ferroelectric integrates this current retaining permanently the image as a charge pattern until readout. A fine grid pattern of electrode lines is deposited on each side of the plate to form rows and columns of a matrix, effectively dividing it into a large number of elemental image points. A two axis commutator is provided for the readout operation. The stored image pattern is scanned by switching the rows and columns in an appropriate sequence. At each switched row/column intersection, the ferroelectric element is discharged, thereby producing an output signal proportional to the stored charges. A detailed description of the Ferrotron concept is given in Appendix A.

The basic principle of line skip commutating is shown in Figure 1a. Here, switches (tags) are "set" during exposure of the image plate which direct during readout the current to only those electrode lines where an element had been illuminated. For example, assuming a star image appears in line 3 and 5, the first readout pulse will flow into line 3 skipping lines 1 and 2. After readout of the element in line 3, switch 3 will be closed, allowing the next readout pulse to flow directly into line 5.

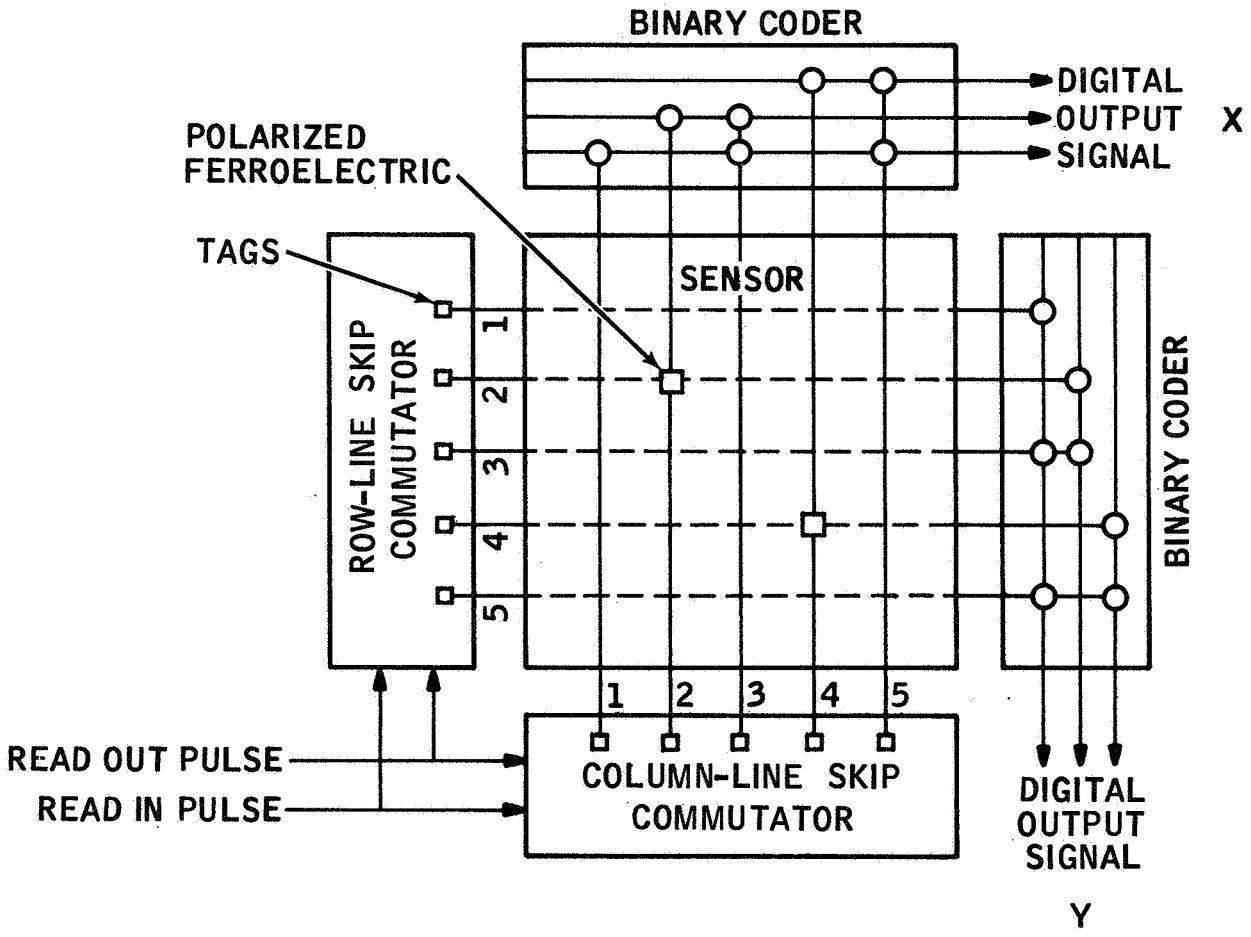
The image transducer plate with line skip feature, Figure 1b, would consist of: (1) the sensor surface with the electrode line grids for the detecting and storing of the image; (2) two line skip commutators, one for each coordinate for scanning the image sensor; (3) the binary encoder for establishing the location data of an illuminated sensor element in binary form.

The commutator contains, in addition to the line scan switches, original location "tags" which are in series with the electrode lines for memorizing those rows and columns that contain illuminated image points.

During exposure, those sensor elements that are illuminated will permit current to flow. This current will polarize the sensor memory elements in a positive direction and simultaneously set the tags in the column commutator. During readout, a pulse is first applied to the column commutator which identifies the location of the first tag and which allows current to flow in the reverse direction through all memorized elements contained in that line, thereby repolarizing them in a negative direction, i.e., erase the stored data, and simultaneously setting the tags of the corresponding row lines. Then, a pulse is applied to the row commutator identifying the location of its first set tag. Thus, the position of an illuminated image point is uniquely determined. A consecutive pulse to the row commutator identifies



A.



B.

Figure 1

PRINCIPLE OF LINE SKIP COMMUTATING

the location of a possible next image point related to the same column. This operation will be continued until all row positions have been identified for that particular column. Then, the next column line containing data is pulsed and the row operation is repeated as above. In this manner, the data contained in the entire image plate is read out with only a few scan pulses.

DESIGN ANALYSIS

System Considerations

The overall functional system of the line skip commutator is shown in Figure 2. The exposure control provides a voltage pulse to the image plate for its activation. As mentioned above, the resultant current at all illuminated image points tags the corresponding columns and image storage element. No data is stored in the row tags.

For readout, the pulse generator energizes the column commutator switching it to its first tag position. Here, the column encoder network is gated for output in binary form. At the same time current is gated to the image storage element and, in turn, to the related row tags. Then, the row commutator register is energized which, in turn, line-skip switches through all tagged stages gating at each stage the row encoder network. Upon completion of the row readout operation the column commutator advances to its next tagged position, thus repeating the cycle until no further signal is detected.

Readout of each tagged column commutator stage clears that particular tag and, as mentioned above, transfers the energy of each ferroelectric image element into its associated row stage, thereby returning that element to its normal state of polarization. Thus, upon finishing a complete scanning operation, the matrix array and all stages of both commutators have been reset and are ready to accept a new exposure.

The implementation of the above line skip readout functions involves the use of digital logic for scanning and a compatible thin film transistor technique.

Logic Functions

In order to have the line skip commutator readout only those points in the image matrix that contain sensed data, the following functions must be provided:

(1) Some form of static storage to remember, for readout purposes, that a ferroelectric element has stored charge. This is necessary since the ferroelectric passes appreciable current only when switching and is thus a dynamic output device.

(2) An encoding network that will provide a binary output to identify specific storage elements that have been set by switching ferroelectrics.

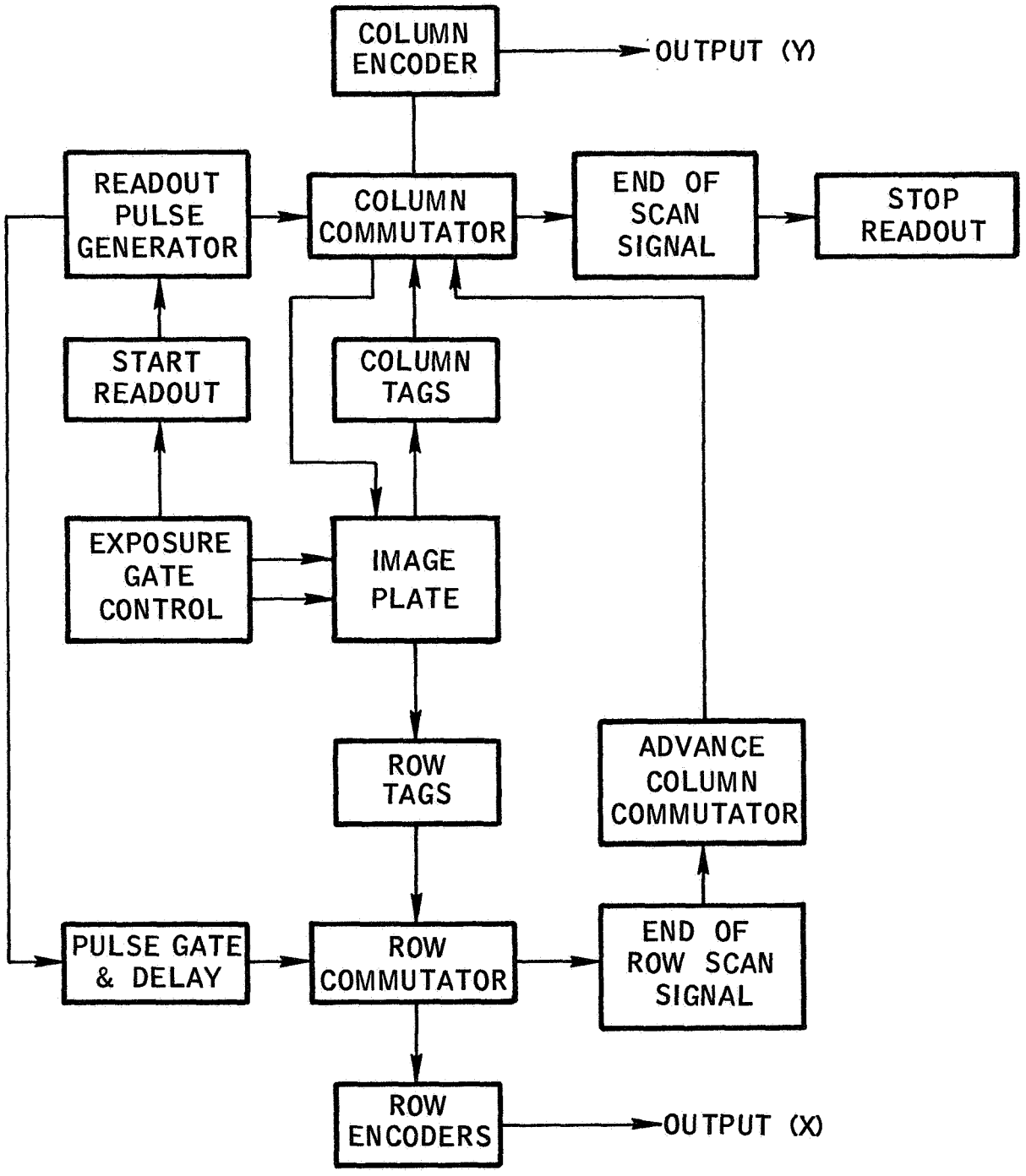


Figure 2

SKIP LINE COMMUTATOR FUNCTIONS

(3) Some form of inhibition such that if a storage element has been set it will inhibit that readout of subsequent elements until it has been read. If the storage element has not been set, its own readout is always inhibited.

(4) Control signals that will read and reset each storage element in the order dictated by the gating logic.

A logic diagram of four stages of a line skip commutator register that incorporates these functions is shown in Figure 3. Flip-flop stages Q_A, Q_B, Q_C, and Q_D provide the static storage and are set during exposure when image data is sensed. Gates G1, G3, G6, and G9 provide readout pulses. Gates G2, G4, G7, and G10 reset their respective flip-flops after readout. Gates G5, G8, and G11 determine, by logic, the next flip-flop for readout during a scanning operation. The logic equations for the gates are:

$$G1 = RO \cdot Q_A \qquad G2 = RS \cdot Q_A$$

$$G3 = RO \cdot \overline{Q_A} \cdot Q_B \qquad G4 = RS \cdot \overline{Q_A} \cdot Q_B$$

$$G5 = \overline{Q_A} \cdot \overline{Q_B} \qquad G6 = RO \cdot G5 \cdot Q_C = RO \cdot \overline{Q_A} \cdot \overline{Q_B} \cdot Q_C$$

$$G7 = RS \cdot G5 \cdot Q_C = RS \cdot \overline{Q_A} \cdot \overline{Q_B} \cdot Q_C \qquad G8 = G5 \cdot Q_C = G5 \cdot \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C}$$

$$G9 = RO \cdot G8 \cdot Q_D = RO \cdot \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot Q_D \qquad G10 = RS \cdot G8 \cdot Q_D = RS \cdot \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot Q_D$$

$$G11 = G8 \cdot \overline{Q_D} = \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D}$$

Use of these equations and the timing diagram in Figure 4 indicates the typical operation of the register. As shown, register stages Q_A and Q_B are set due to the presence of image data on their matrix input lines during exposure of the image plate. The positive condition of Q_A and the presence of a read pulse (RO) activates gate G1 which furnishes a pulse to the encoding network for binary output. A reset pulse (RS) is applied to the control line which activates gate G2 and thus resets flip-flop Q_A. Gate G5 is activated by the reset condition of Q_A and Q_B. The next read pulse on the control line, in conjunction with the output of gate G5 and the set condition of Q_C activates gate G6 providing a binary encoded output for Q_C. The next reset pulse (RS) resets flip-flop Q_C through gate G7. This reset condition activates gates G8 and G11. The next readout pulse (RO) would be logically gated to the next flip-flop in the register which had been set by image data.

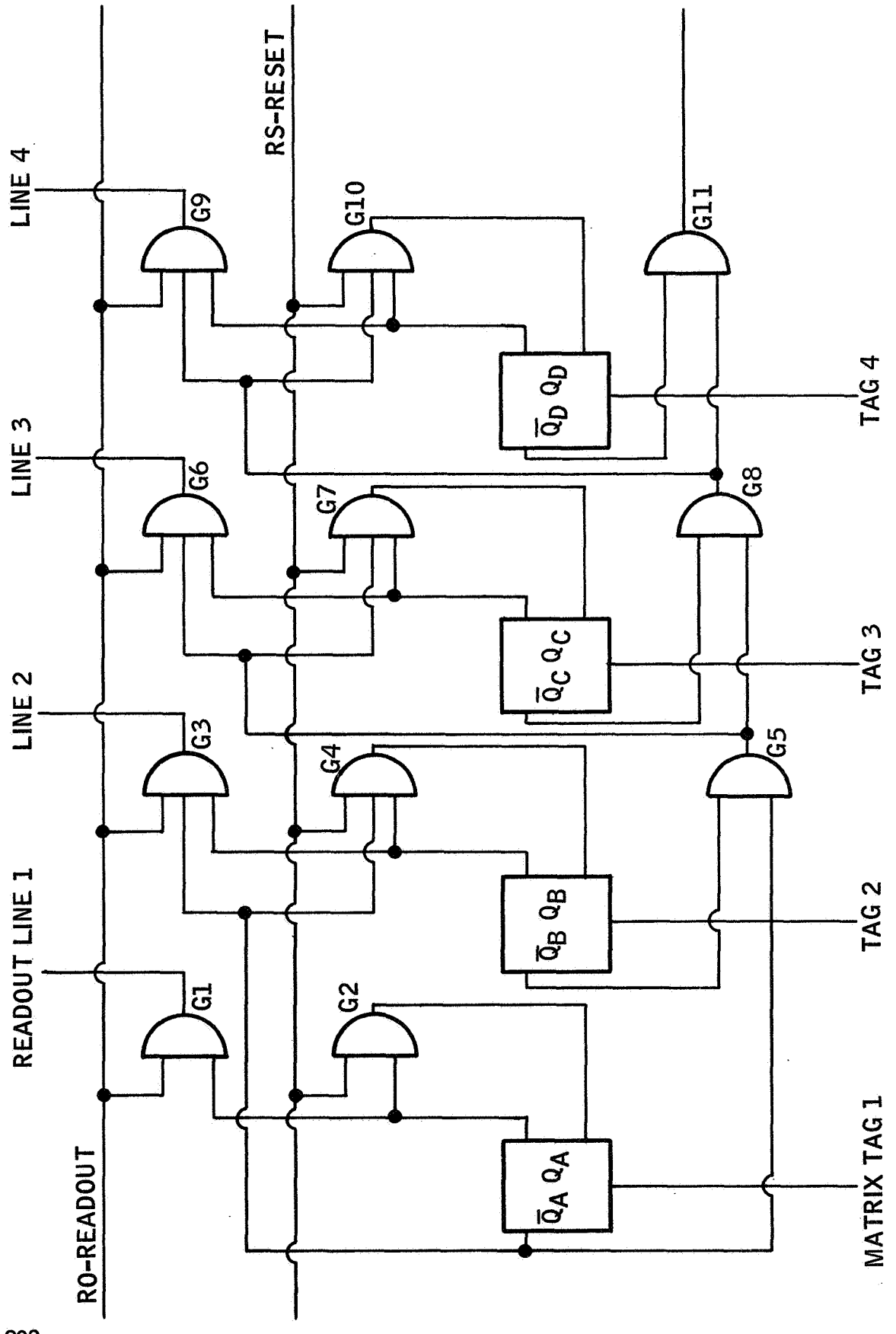


Figure 3

LOGIC BLOCK DIAGRAM - LINE SKIP COMMUTATOR

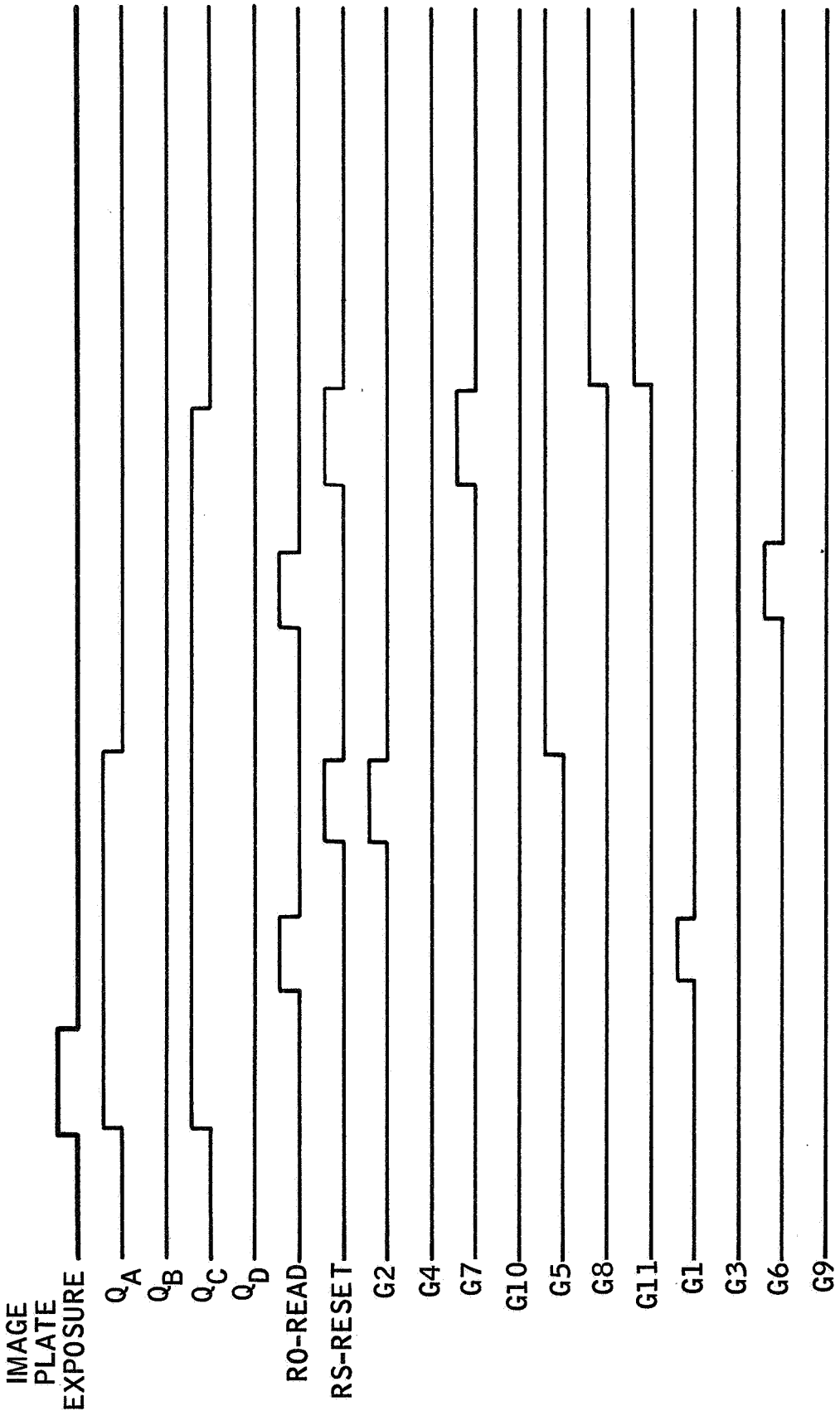


Figure 4

TIMING DIAGRAM - LINE SKIP COMMUTATOR

Thin Film Elements

The thin film transistor (TFT) is essentially a field effect device in which the conductivity of a semiconductor is modulated by the application of a transverse electrical field. (The geometry of such a device is shown in Figure 5). Current flow in the device is initiated by a voltage between the source and drain electrodes. Under these conditions, the application of voltage to the insulated electrode, or gate, induces a charge into the semiconductor which attracts a proportional number of carriers from the source electrode. Thus the applied field has an effect on the conductivity of the device.

For example, with a positive gate potential, positive charges on the electrode side of the insulator induce a corresponding negative charge at the semiconductor side. As the voltage increases, the positive charge at the gate is increased and the negative charge in the semiconductor is increased with a proportional increasing change in the conductivity. The current flow from the drain to the source thus will be "enhanced" by the applied gate potential and the device is said to work in the "enhancement" mode. An increase of a negative gate voltage decreases the gate current in the "depletion" mode.

With a zero voltage on the gate, an ohmic current, I_{do}, will flow from the drain to the source for an n-type semiconductor material. The magnitude of this current will depend upon the resistivity of the material. Small intrinsic free carrier densities can be realized by the use of semi-insulators, or wide band gap materials such as cadmium sulfide-cadmium selenide (CdS-CdSe). When low signal levels such as those derived from solid state image plates, are used, this requirement becomes very important.

Examination of the equation for the saturated drain current at zero gate bias

$$I_{do} = \frac{u N_o^2 e^2}{2 L^2 C_g}$$

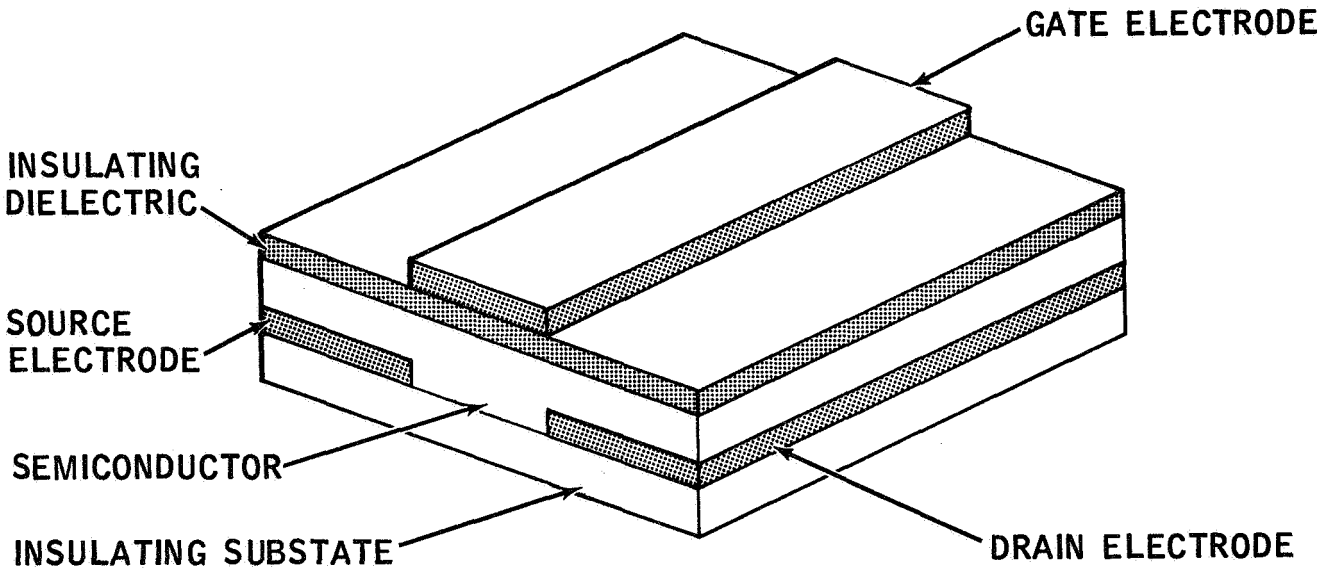
where u = drift mobility in $cm^2 volt^{-1} sec^{-1}$

N_o = density of surface states

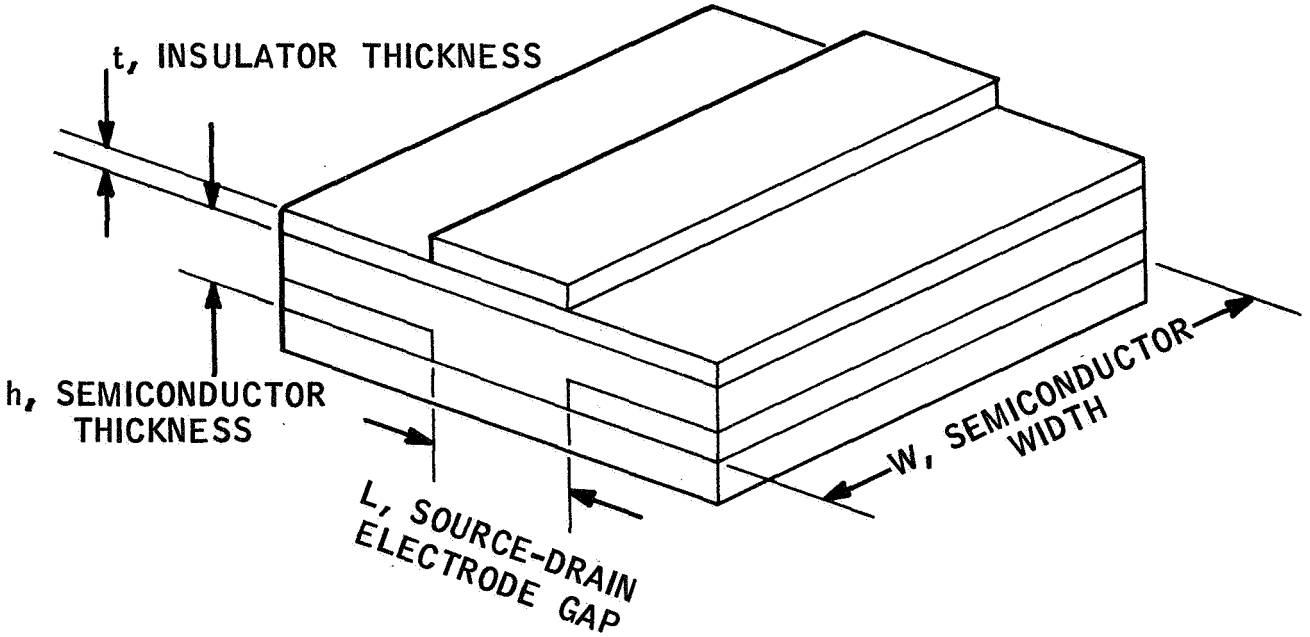
e = electron charge, 1.6×10^{-19} coulombs

L = source drain gap width, cm

C_g = input gate capacitance in farads



(A) TFT STRUCTURE



(B) DIMENSIONAL PARAMETERS

Figure 5

TFT GEOMETRY

To make I_{do} as small as possible for a given resistivity material the thickness of the semiconductor, h, should be reduced to make N_o small and the thickness of the insulator, t, should be reduced to make C_g large as possible.

Another important parameter of the TFT is V_o, the gate threshold voltage necessary for conduction in the semiconductor. (Disregarding I_{do})

$$V_o = \frac{eN_o WL}{C_g}$$

Since the gate capacitance, $C_g = \frac{KWL\ 10^{-12}}{4\pi t^2}$, a substitution can be made

$$V_o = \frac{eN_o WL}{KWL\ 10^{-12}} \cdot \frac{4\pi t^2}{1}$$

This second form of the equation shows that for a given insulation material (given K), the threshold can be minimized by making N_o and t small.

In order to realize maximum gain from the TFT, it is desirable to make the transconductance, g_m, as large as possible. The equation for g_m is

$$g_m = \frac{uC_g(V_g - V_o)}{L^2}$$

With a given drift mobility, u, the transconductance can be increased by making L as small as possible. (C_g decreases linearly with L but W can be increased to compensate for the change).

A large capacity high resolution image plate requires a high resolution commutator implementation. From the above observations, it can be seen that a small L, or source drain electrode spacing provides this compatibility since this dimension essentially governs the resolution in one axis.

The use of ion implantation techniques (as discussed in the next section) can fulfill the requirement for a very thin insulation layer, t. In addition, the use of this technique can provide the very narrow TFT electrodes necessary to achieve the desired high resolution.

To provide an estimate of the characteristics of a high resolution TFT that could be deposited on the same substrate as a solid state image sensor, a 1 mil by 1 mil device can be assumed with a 4 micron source-drain gap. A

drift mobility value of 150 $cm^2 volt^{-1} sec^{-1}$ is characteristic of a Marquardt developed CdS-CdSe material which would serve as the semiconductor. An insulator material consisting of Be_2O_3, Dy_2O_3, and SiO_2 has a dielectric constant of 4.5 and a breakdown voltage exceeding 3×10^6 volts cm^{-1}. A gate insulator thickness, t, of 100°A would require operation below a 3 volt level which should be more than satisfactory for a low level digital logic requirement. Assuming these values, the gate capacitance would have a value of

$$C_g = \frac{KWL\ 10^{-12}}{4\pi t}$$

$$= \frac{4 \times 2.5 \times 10^{-3} \times 4 \times 10^{-4} \times 10^{-12}}{4\pi 10^{-6}}$$

$$= 3 \times 10^{-13} \text{ farad}$$

The transconductance, g_m, assuming a negligible threshold voltage, would be

$$g_m = \frac{uC_g V_g}{L^2}$$

$$= \frac{1.5 \times 10^2 \times 3 \times 10^{-13} \times 2}{16 \times 10^{-8}}$$

$$= 660 \text{ microamperes volt}^{-1}$$

The gain-bandwidth

$$GB = \frac{g_m}{2\pi C_g}$$

$$= \frac{6.6 \times 10^{-4}}{2\pi 3 \times 10^{-13}}$$

$$= 320 \times 10^6 \text{ hertz}$$

A line skip commutator implemented by elements exhibiting these characteristics would be satisfactory for selective readout of an image sensor plate.

MATERIAL FOR SWITCHING ELEMENTS

The implementation of the line skip commutator logic functions requires switching elements that are compatible with the electrical and physical characteristics of the sensor elements. The use of thin film transistors offers several advantages over integrated circuitry and MOS insulated gate field effect transistors (IGFET) implementations. For example: Conventional integrated circuitry cannot provide the required high resolution or packing density. The MOS-IGFET implementation could possibly overcome this limitation. In addition, its high input impedance would permit a high loading or fanout ratio which is a desirable feature in digital logic circuitry. It also could be made to exhibit a threshold voltage which improves noise immunity.

However, the fabrication process of MOS-IGFET's is not compatible with that of the image sensor. It requires a silicon material involving a separate diffusion process and a complex interconnecting scheme. Also, the silicon is a relatively narrow band gap material exhibiting a too low resistivity when using it in conjunction with the ferroelectric material in the image sensor.

In contrast, the thin film transistor (TFT) can be deposited directly onto the image sensor substrate because it is composed of the same material, i.e., cadmium sulfide. The electroding and diffusion operation can be performed simultaneously for both materials. Furthermore, the thinness of the semiconductor layer that is possible with deposition techniques enhances the gate control characteristics of the TFT. Since there is also electrical compatibility with the sensor element as analyzed in the previous section, the TFT is considered best suited for the implementation of switching elements for the contemplated line skip commutator.

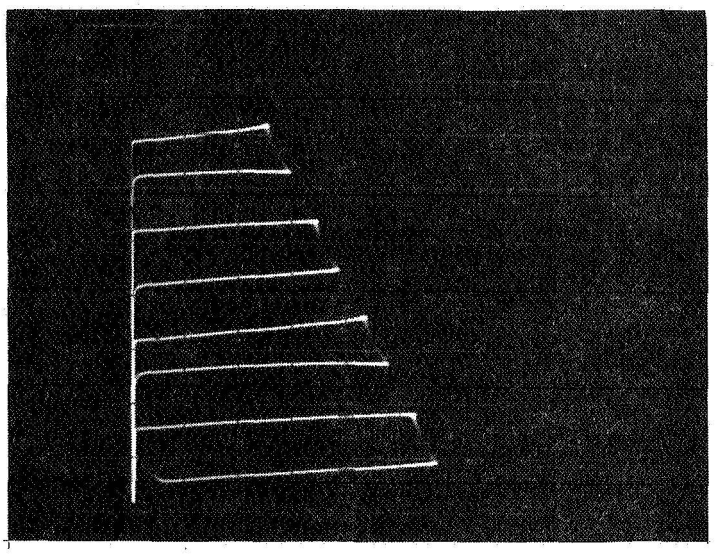
The TFT requires for its fabrication both a semiconductor host material and a gate insulating material. For the preparation of the host material, the process Marquardt has developed under other programs for the deposition of thin film cadmium sulfide photoconductive materials is applicable. It consists of depositing at low substrate temperature an amorphous material which is post heat treated to obtain crystallinity. The low temperature minimizes the creation of vacancy defects and permits precise control of the material parameters. This material being a II-VI compound offers the wide band gap desired for obtaining high resistivity and provides at the same time a satisfactory value of drift mobility.

A gate insulating material was investigated during this program for compatibility with the above semiconductor material. Its characteristics must be such that it does not strain the material film, i.e., it must have

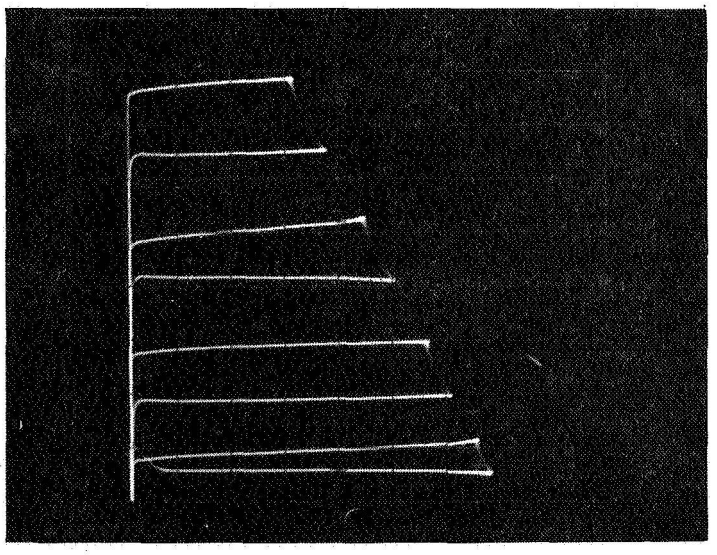
an equal expansion coefficient with the cadmium sulfide. It must be chemically stable and not react with the semiconductor as in the case when employing the usual alkali fluxes. The ionic contribution in the insulator lattice must be small when considering the high resistivity characteristic of the cadmium sulfide semiconductor host material.

The insulator material that was developed is basically a borosilica glass with a rare earth acting as a lattice modifier and consists of boron oxide, dysprosium oxide, and silicon dioxide. (B_2O_3, Dy_2O_3, and SiO_2). Films of this insulator material were produced by flash evaporation which met the above requirements. For example: The coefficient of expansion is 4.6×10^{-6}cm cm^{-1} $^oC^{-1}$ which is close to that of intrinsic cadmium sulfide with 4.5×10^{-6}cm cm^{-1} $^oC^{-1}$. The dielectric constant has been measured as 4.5 which is acceptable for this application as indicated in the analysis section.

A number of thin film transistors have been fabricated using indium electrodes for the drain and source with a gold electrode over the insulator material. Experimental evaluation indicated typical transconductance values of 5000 microamperes per volt. See Figure 6 for typical voltage - current characteristics. Under another program, several thin film shift registers were implemented to test device operation. The successive thin film layers were vacuum deposited on glass substrates. Chromium electrodes were used to provide the source, gate, and drain geometries. Transconductance values of 2000 microamperes per volt were measured for the individual elements. Experimental evaluation was limited due to drift problems encountered during commutator operation.



HORIZONTAL: 2 VOLTS/DIV.
VERTICAL: 20 μA/DIV.
GATE CURRENT: 20 μA/STEP
DRAIN LOAD: 50K OHMS



HORIZONTAL: 2 VOLTS/DIV.
VERTICAL: 20 μA/DIV.
BASE CURRENT: 2 μA/STEP
COLLECTOR LOAD: 50K OHMS

Figure 6

CHARACTERISTIC CURVES OF TMC TFT AND 2N696 TRANSISTOR

HIGH RESOLUTION DEPOSITION TECHNIQUES

As discussed above, the readout of high resolution image transducers requires the fabrication of thin film circuitry with very high element packing density. The use of ion implantation techniques provides an approach that can realize this desired resolution.

Theory

Ion implantation is a process in which energetic ions are introduced into and retained in a host crystal. As such, any ion can be implanted in any material thus providing a unique method of doping compound semiconductors. Since the process can take place at temperatures below 600°C, many of the problems commonly associated with diffusion processes are eliminated. For example, the number of defects produced by the processing can be reduced considerably.

The passage of the energetic ion through the host crystal creates vacancies and interstitials which form various defect species around the path of the ion. When the host crystal is annealed to remove this damage, the dopant ions move to substitutional or interstitial sites and the defect species dissociate and diffuse. The annealing temperature is kept low to insure a small region of migration in the neighborhood of the implanted ions.

Ion implantation is based on the generation and control of a stream of ionized atoms of the desired element which is accomplished by (1) vaporization of the element by conventional vacuum heating techniques, (2) ionization of the resultant vapor flow by means of the atoms impinging on a heated cathode, (3) the generation of a stream of ions with a known velocity and distribution that is directed from the cathode into an ion optical system, (4) the acceleration and focussing of the ion beam onto a host crystal for implantation, and (5) annealing of the host crystal to produce migration.

Many ionization techniques can be used for the production of the desired ions, for example, surface ionization and electron impact ionization. Elements with ionization potentials below about 6 e.v. can be produced by surface ionization, e.g., In, Ga, Al, Th, the lanthanide rare earths, and the alkali metals. Elements with higher ionization potentials but moderate heat of vaporization can be ionized by electron impact, e.g., P, As, Te, Ze, Cd, Sb, Hg, and Se, Au and Ag with higher heat of vaporization may be handled in other ways.

A most important characteristic in the ion implantation process is the determination of the ionizing surface temperature at which a given ion current density is obtained for a particular ion beam and heated substrate combination.

For example, a temperature of 1600 to 1800°K is required with an iridium surface to produce a current of indium ions in a range of 0.1 to 10 micro-amperes cm^{-2} while 1800 to 2000°K would be required for aluminum. This indicates why highly refractory materials are required to obtain desired current densities, since the ionizing surface must not contribute any atoms of its own by the partial vapor pressure it would provide at the ionizing temperature.

The ionization efficiencies can be calculated by the Saha-Langmuir equation.

$$\beta = \left[1 + \left(\frac{W_o}{W_4}\right) \exp\left(\frac{I - \phi}{kT}\right)\right]^{-1} \quad \text{when } T > T_c$$

with, T_c, the critical temperature, simplifying further

$$\beta = \exp -F \ (I - \phi) \ /RT$$

which gives the ratio of atoms impinging on the hot surface and re-evaporating either as neutral atoms or as positive ions per second. With, I, the ionization potential, ϕ, the work function of the heated surface, and F, the Faraday number in the above equations. Thus with $(I - \phi) \sim -0.5$ volts, all of the atoms evaporate as ions.

Implantations of these ions can be achieved with satisfactory current densities with beam extraction potentials in a range between 50 volts to 5000 volts. The ion beam may be accelerated and focussed by an ion-optical system in all respects similar to conventional electron-optics. See Figure 7.

Considering the limitations imposed on the focussing of ion beams to a very small spot size, the limitations imposed by space charge, spherical aberration, and thermal velocities must be taken into account.

As a result of space charge expansion, the minimum spot radius, r_m, is related to the beam parameters as

$$\ln \frac{r_m}{r_o} = - \frac{a^2}{(174)^2 \left(\frac{m_i}{m_c}\right)^{1/2} P_i}$$

where P_i = ion beam perveance $\dfrac{J_i}{V_o^{3/2}}$

a = initial convergence angle of the ions emerging from the focussing lens

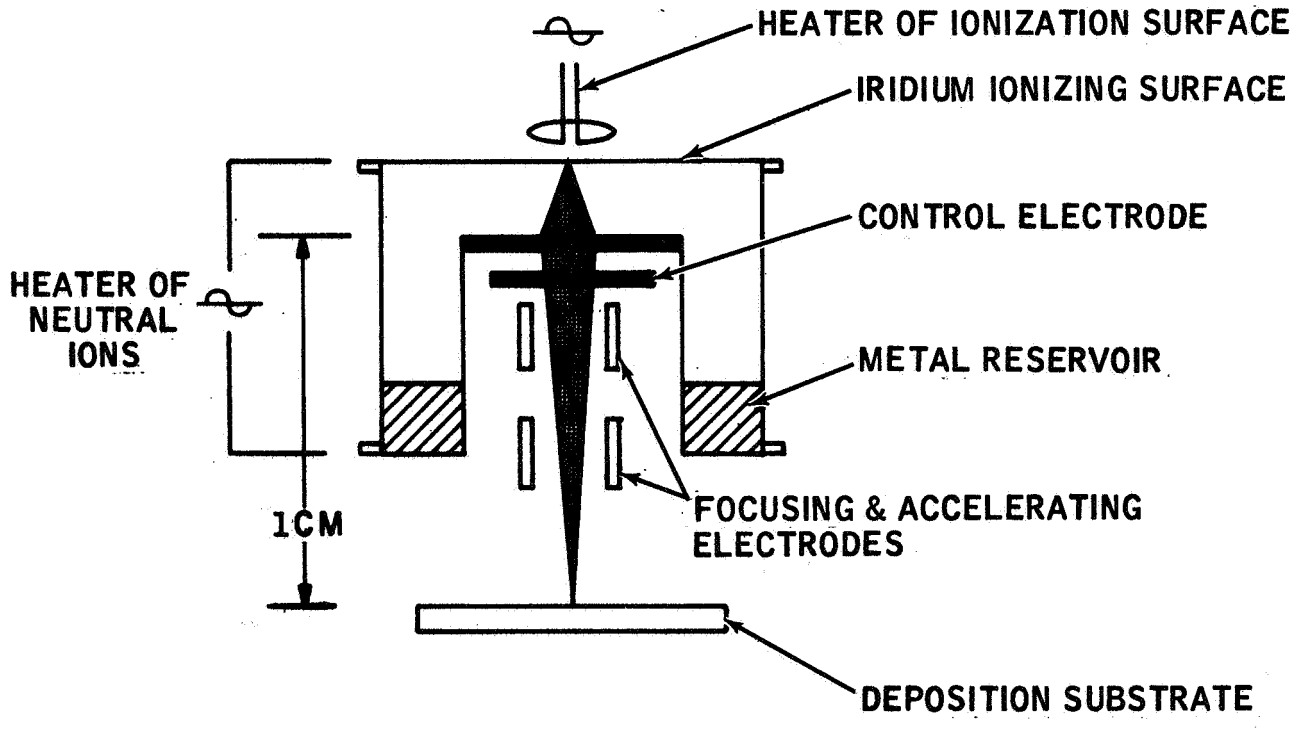


Figure 7

ION BEAM IMPLANTATION SCHEMATIC

R-22,600

r_o = initial beam radius

The maximum current density which can be focussed into a spot is from the above equation, given by

$$J_i = \frac{a^2 V_o^{3/2}}{(174)^2 \left(\frac{m_i}{m_c}\right)^{1/2} \pi r_m^2 \ln \frac{r_o}{r_m}}$$

which can be expressed in terms of temperature and pressure

$$I_i = \frac{N_o}{(2\ \pi RMT)^{1/2}} \quad \frac{pa_o}{\pi r^2} \quad \text{molecules cm}^{-2}\text{sec}^{-1}$$

where N_o = Avrogadro's number

R = Gas constant for mole

M = Molecular weight

p = dynes cm^{-2}

a_o = Area of source orifice

With indium ions focussed with an initial convergence of about 17^o, i.e., a = 0.3, a spot size of 1 micron can be achieved at an accelerating potential of 100 volts with a beam current of 10^{-6} amperes. Thus, it is obvious that the desired spot size will not be limited by space charge beam divergence.

Another limitation in spot size may result from spherical aberration, i.e., the tendency of the lens system to focus ions at the periphery of the beam rather than the ions near the axis. Since ions will cross the axis at different axial positions, there would not be a place of sharp focus. At the plane where the beam exhibits a minimum diameter 2h, i.e., the disc of least confusion which is given by Klemperer as

$$h = \frac{C_s}{4} \theta^3$$

With C_s, the spherical aberration coefficient, and θ, the angle of convergence, taking from Klemperer the example of a symmetrical two cylinder electrostatic lens, gives

$$C_s = R$$

with R, the radius of the lens tube and with a voltage ratio of 18 to 1. the minimum spot size will be

$$h = \frac{R\,\theta^3}{4}$$

using, for example, θ = 0.04 radians, and R = 1 centimeter

$$h = 0.16 \text{ microns}$$

This spherical aberration does not impose limitations to a micron size spot.

Ions emerge from the source, either from contact of plasma ionization with a Maxwellian distribution of transversal velocities, i.e., the edge will become diffuse rather than sharp.

In selecting the ions with certain initial velocities, one limits the current density arriving at the focussed spot, J_m, to a value inferior to the current, J_o, from the source. From Langmuirs equation

$$J_m = J_o \frac{dV_o}{kT} \sin^2 \theta$$

Thus, the effect of a finite transverse velocity of the ions will be a limitation on the current density achievable in a small spot.

The largest possible ratio between the two currents combining Langmuir's and spherical aberrations and letting the spot size be equal to the disc of least confusion, $2h = d_s$.

$$\frac{J_m}{J_o} = \frac{eV_o}{kT} \theta^2 \frac{1.16 \times 10^3}{T} V_o \left(\frac{2ds}{R}\right)^{2/3}$$

Assuming that 10^{15} ions $cm^{-2} sec^{-1}$ are needed at the surface of implantation, i.e., a current density of 10^{-4} ampere cm^{-2} in a spot d_s=1, with V_o = 10KV; R = 0.5 cm, and T = 1160°K, the ratio becomes

$$\frac{J_m}{J_o} = 10^5 \, (0.4 \times 10^{-3})^{2/3}$$
$$= 5 \times 10^4$$

Thus, in order to obtain a current density of the focussed spot $J_m = 10^{-4}$ amperes cm^{-2}, the current density of the source J_o has to be greater than 2×10^{-7} amperes cm^{-2}.

Experimentation

In order to provide the correct environment for the ion implantation studies, a special ultra-high vacuum (a Varian VT - 105) station was retooled partly in conjunction with another program. This station is shown in Figure 8.

A design study was conducted to provide the ion beam "gun" which implements the various functions of the ion implantation process as described above. This gun consists of a material reservoir and heater, ionization plate and heater, accelerating and focussing electrodes, and support structure. The components and a partial assembly are shown in Figures 9 and 10. The assembled system is shown in Figure 11. In operation, a selected material is vaporized in the material reservoir and then surface ionized on the heated ionization plate (an iridium disk). The resulting free ions are accelerated toward the host material which is to be doped with the desired energy of impact and focussed to a micron sized spot at the nominal Z position of the substrate stage. This equipment was fabricated, assembled, and installed in the ultra-high vacuum station. In addition, a sensor gauge for use with a mass spectrometer was mounted on the vacuum chamber.

During the course of the design it was found necessary to design special bifilar coils for the reservoir and ionization plate heaters. The heater configurations are both bifilar to minimize stray fields which can influence the motion of the ionized atoms during acceleration. One heater was a flat iridium strip in the shape of an S and the second heater configuration was a bifilar edgewound coil of flat iridium strip. Calibration data for the ionization plate temperature versus heater coil current is shown graphically in Figure 12 for the two heater configurations.

One of the very basic calibration tests for the implantation process is to establish the evaporation constants of the material to be implanted as a function of the evaporation temperature under high vacuum conditions. The material reservoir and the ionization plate temperatures are monitored by heater current as discussed above. Indium metal was selected as the first metal to be investigated because it has a relatively low temperature of vaporization in low vacua, i.e. 10^{-5} to 10^{-9} torr and a relatively low temperature of ionization, i.e. 1100 to 1400°C. As a next step, the types and amounts of the various ionized species emitted by the ion gun are measured using a mass spectrometer. However, during these tests, the ionization heater coil burned out at an elevated temperature.

To eliminate this heater problem, it was decided to use an electron beam heater rather than the resistive heating techniques discussed above. For this purpose, the ion gun was redesigned to adapt a commercially available

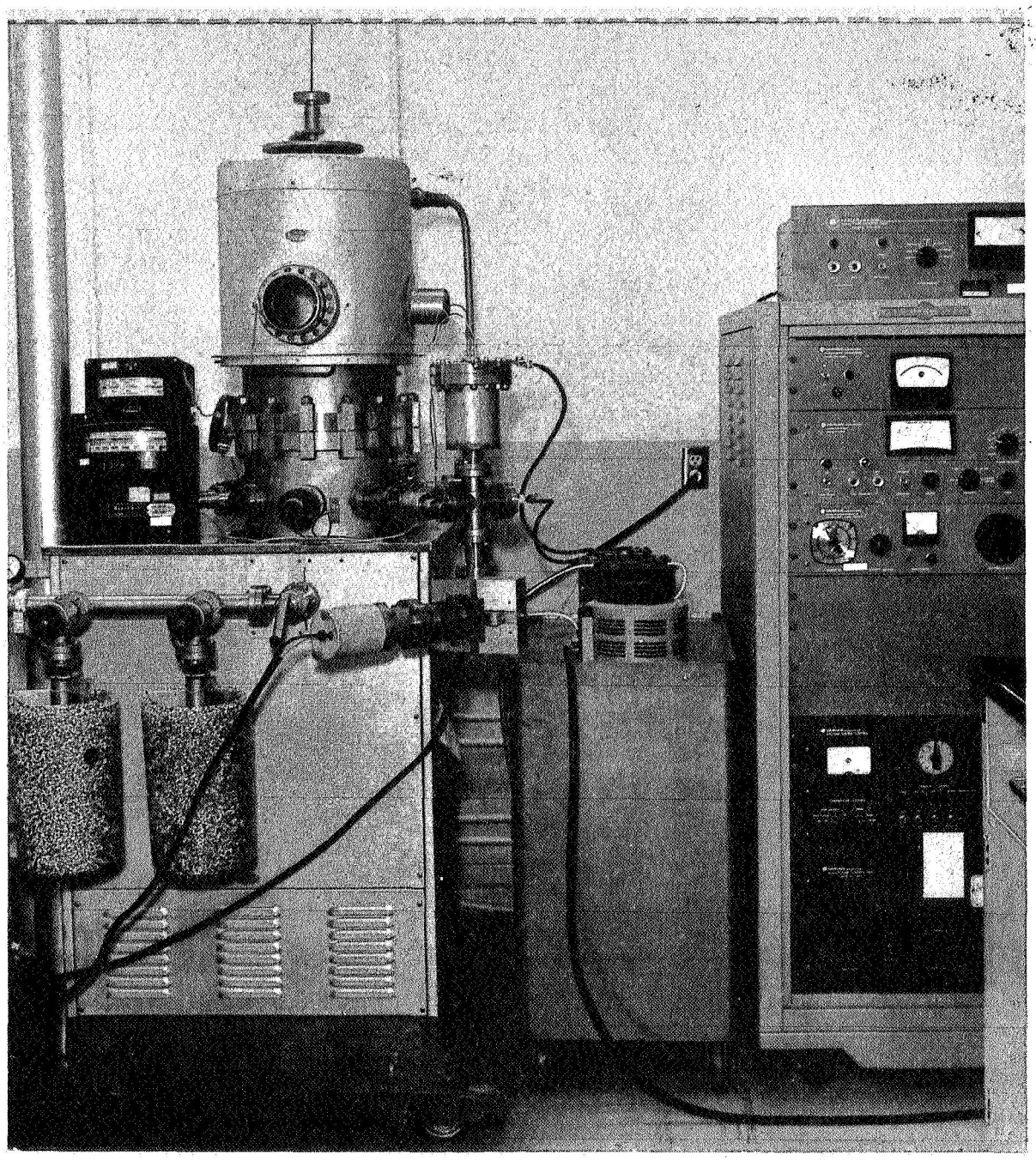


Figure 8

ULTRA HIGH VACUUM STATION AND CONTROL PANELS

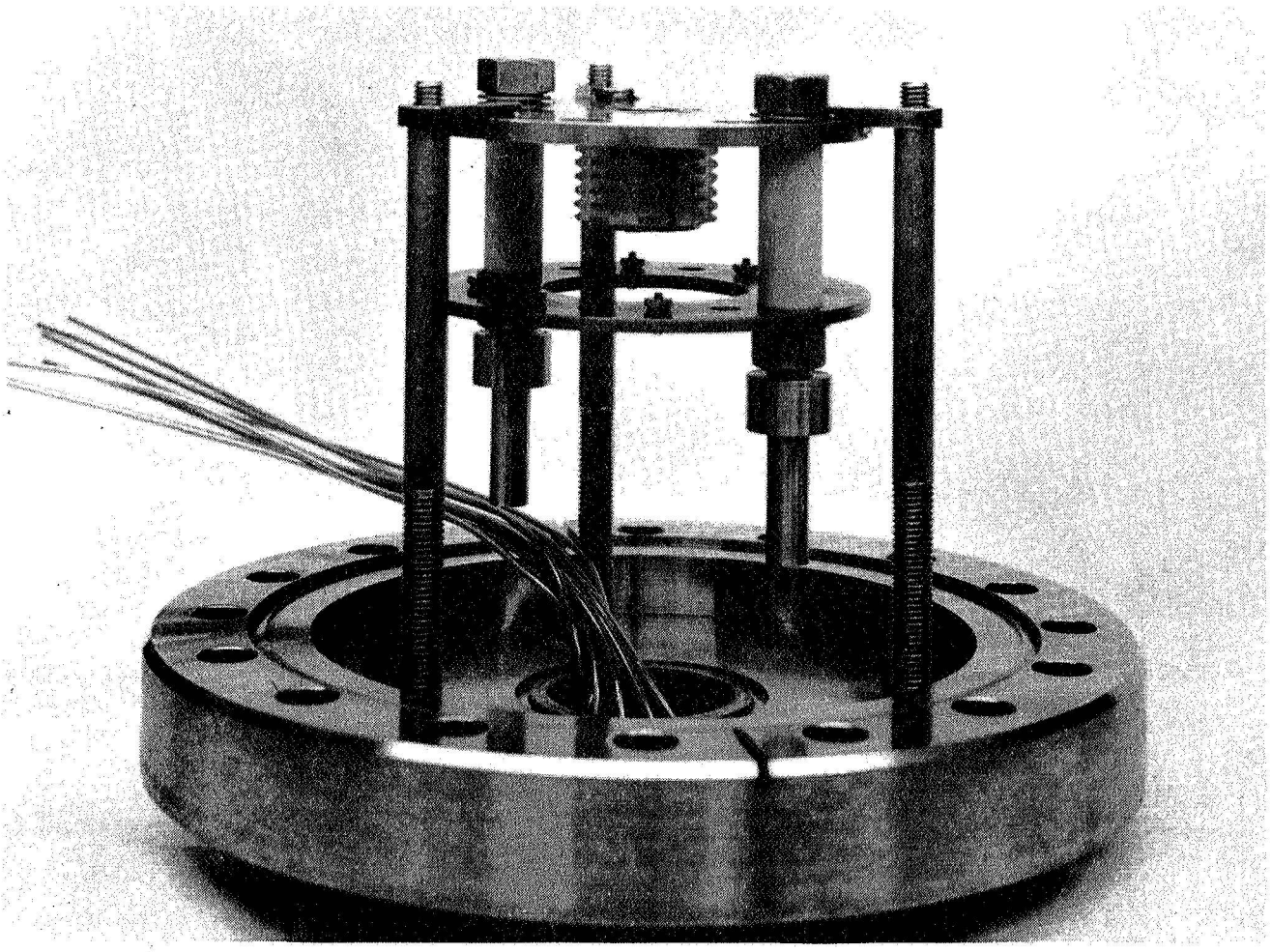


Figure 9

ION IMPLANTATION GUN
FUEL RESERVOIR REMOVED

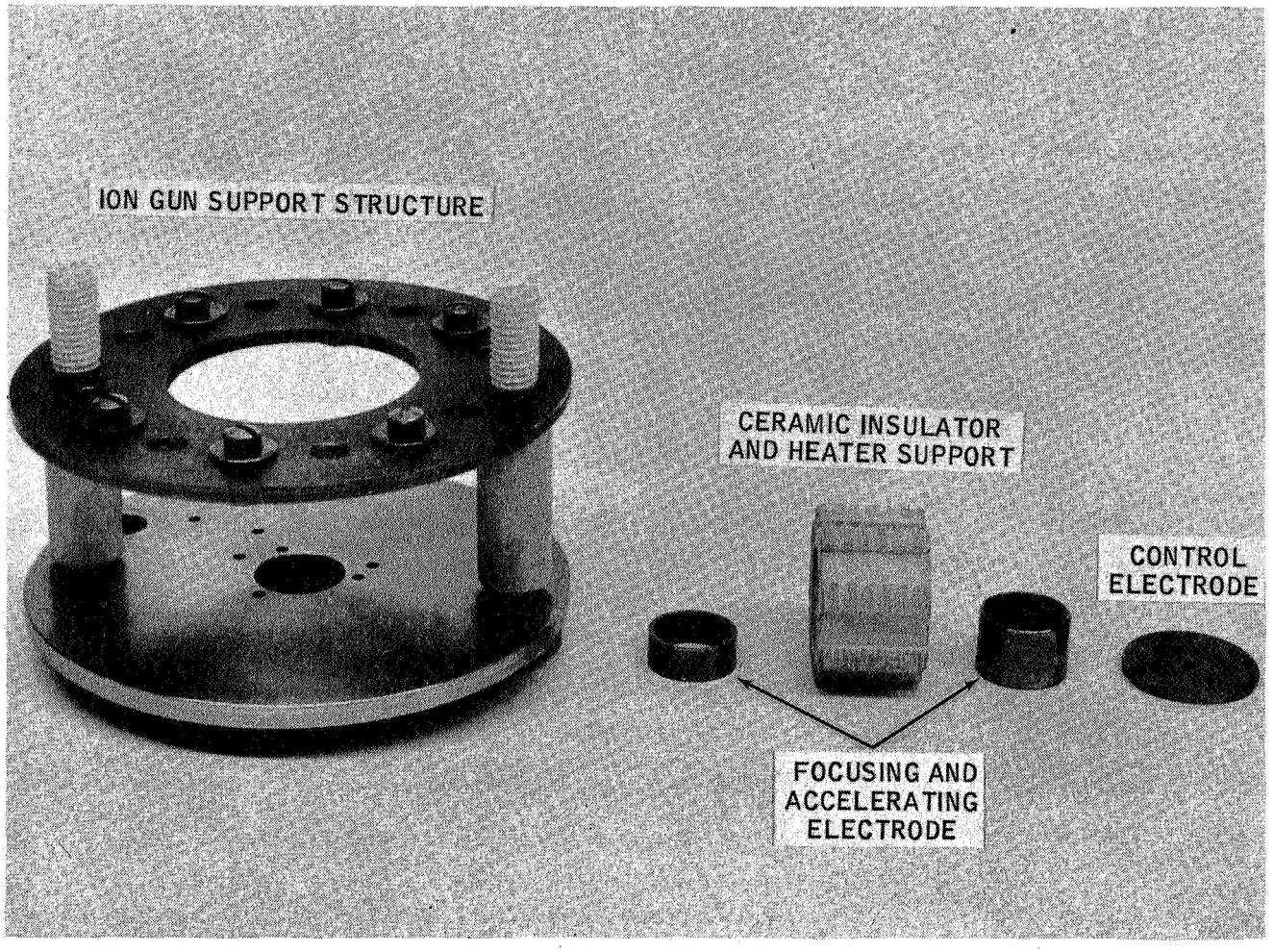


Figure 10

EXPLODED VIEW OF ION GUN

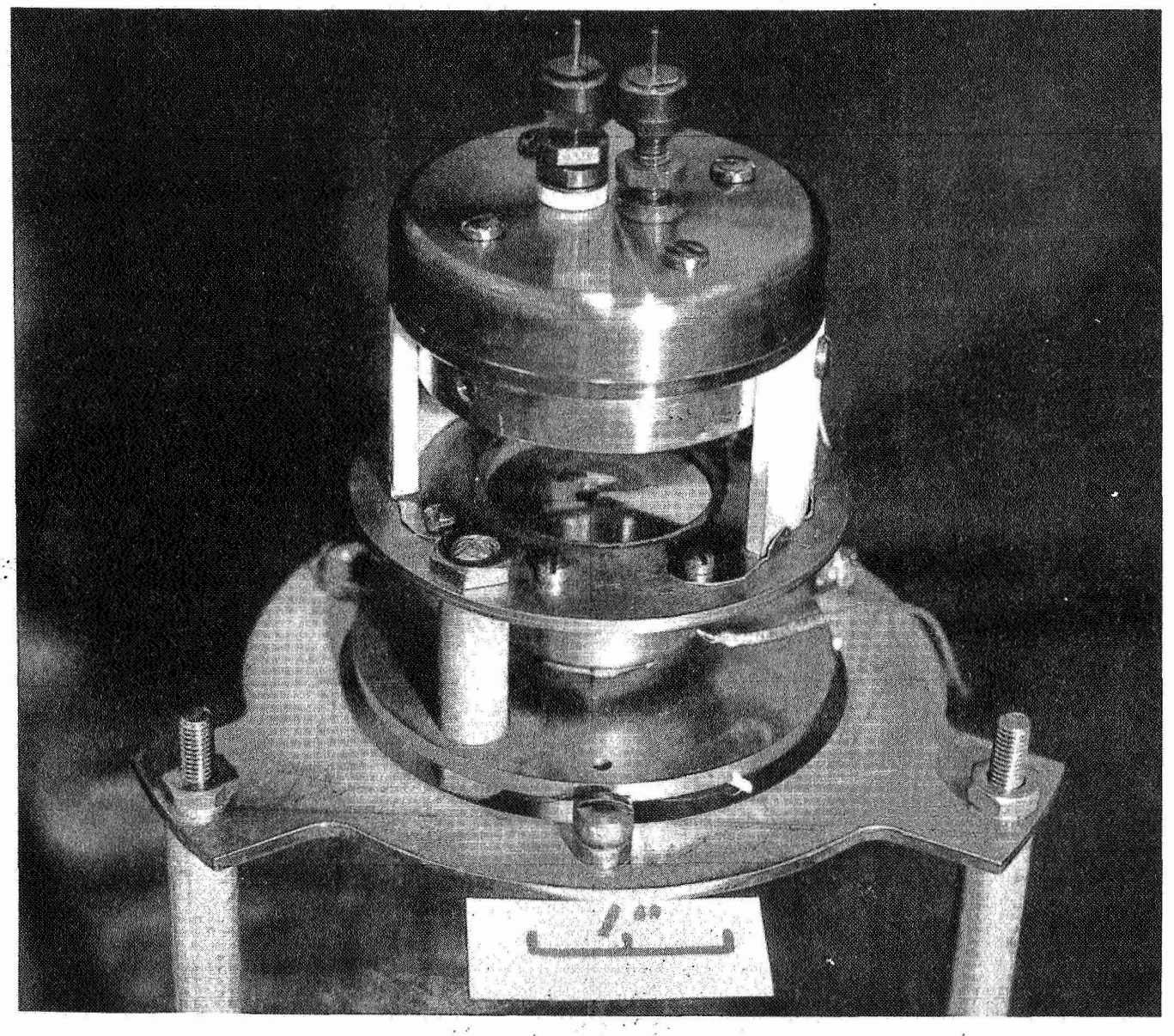


Figure 11
ION GUN ASSEMBLAGE WITH ELECTRON BEAM HEATER

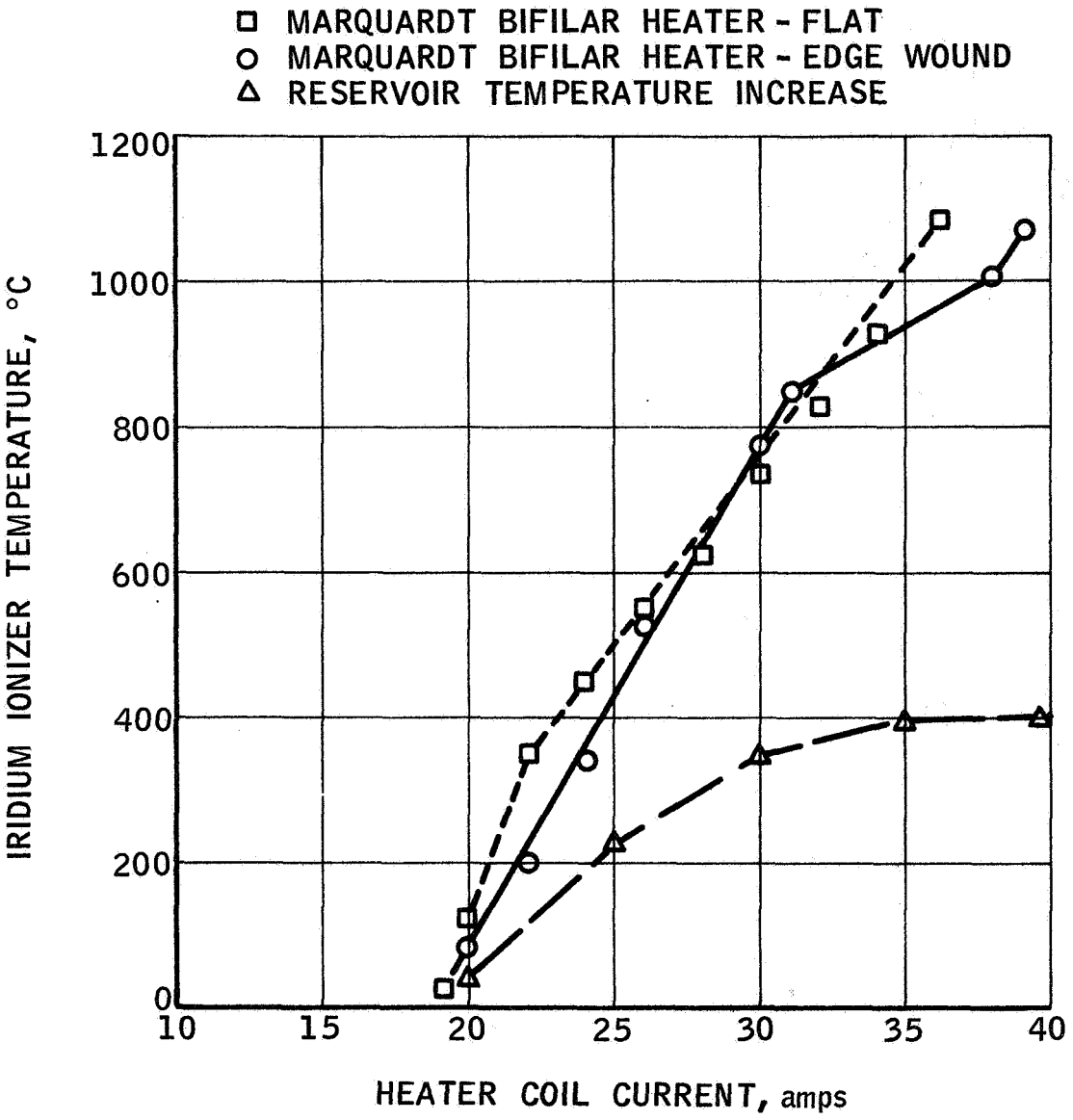


Figure 12
IONIZATION PLATE HEATER COIL
TEMPERATURE/CURRENT RELATIONSHIP

Pierce-type electron gun made by Veeco Instruments, Inc. (VeB-6). It is a self-accelerated, electrostatically focussed beam gun which concentrates a maximum of 6 kilowatts of energy on a 1/8th inch diameter spot. The focussing electrodes for the electron gun were removed to allow the electrons to be formed into a larger than normal beam size by the accelerating voltage (4KV). With this work completed it was possible to achieve ionization plate temperatures above 1900°K over an area of approximately one inch in diameter.

The preparation of the specific commutator circuitry with the above ion implantation technique requires a mechanism inside the vacuum machine to move the ion beam over the substrate in a precise pattern. A three axis control has to be provided where the Z-axis adjusts the focus of the beam to obtain a specific line width on the substrate at the point where the X-axis indexes and the Y-axis scans the substrate laterally. As indicated in the design analysis section, the dimension of a switching element is in the order of 1 mil and the width of the electrodes within this area is 0.3 mils or approximately 8 microns. For reasons of performance uniformity, the planting of these electrodes should be done with a precision of 1 mil or better. The feasibility of accomplishing such an accuracy over an area as large as the contemplated image sensor was investigated. It was found that conventional methods of deflecting the beam electronically are not suitable because of inherent distortion and non-linear performance characteristics. A mechanical method based on standard linear actuators for feeding the two lateral motions through the vacuum chamber as indicated in the preliminary design of Figure 13 would offer a better linearity over the desired area, but cannot produce a sufficient positional accuracy. In this method, the two motions interfere with each other because each mechanism is referenced separately to the vacuum machine base ring. Also, tests with the standard actuators showed a backlash of 100 microns which would be difficult to reduce to an acceptable value.

A second mechanical design concept that overcomes the above shortcomings is shown in Figure 14. Here the two motions are referenced to each other by superimposing the Y-scanning mechanism upon the X-indexing mechanism, which, in turn, is referenced to the base ring. Both motions are accomplished through the same porthole by a special mechanism that integrates both actuations. An added advantage is offered by the possibility of operating this mechanism through bellows which reduces the effect of vacuum deterioration when using standard actuators. A preliminary analysis indicated that the desired accuracies can be obtained with this approach provided appropriate consideration is given to the vibration field and the temperature distribution in the vacuum chamber.

In preparation for the initial ion beam experiments, a less accurate and simpler one axis mechanism was installed in the high vacuum machine utilizing a micrometer stage for its construction. It provides the means

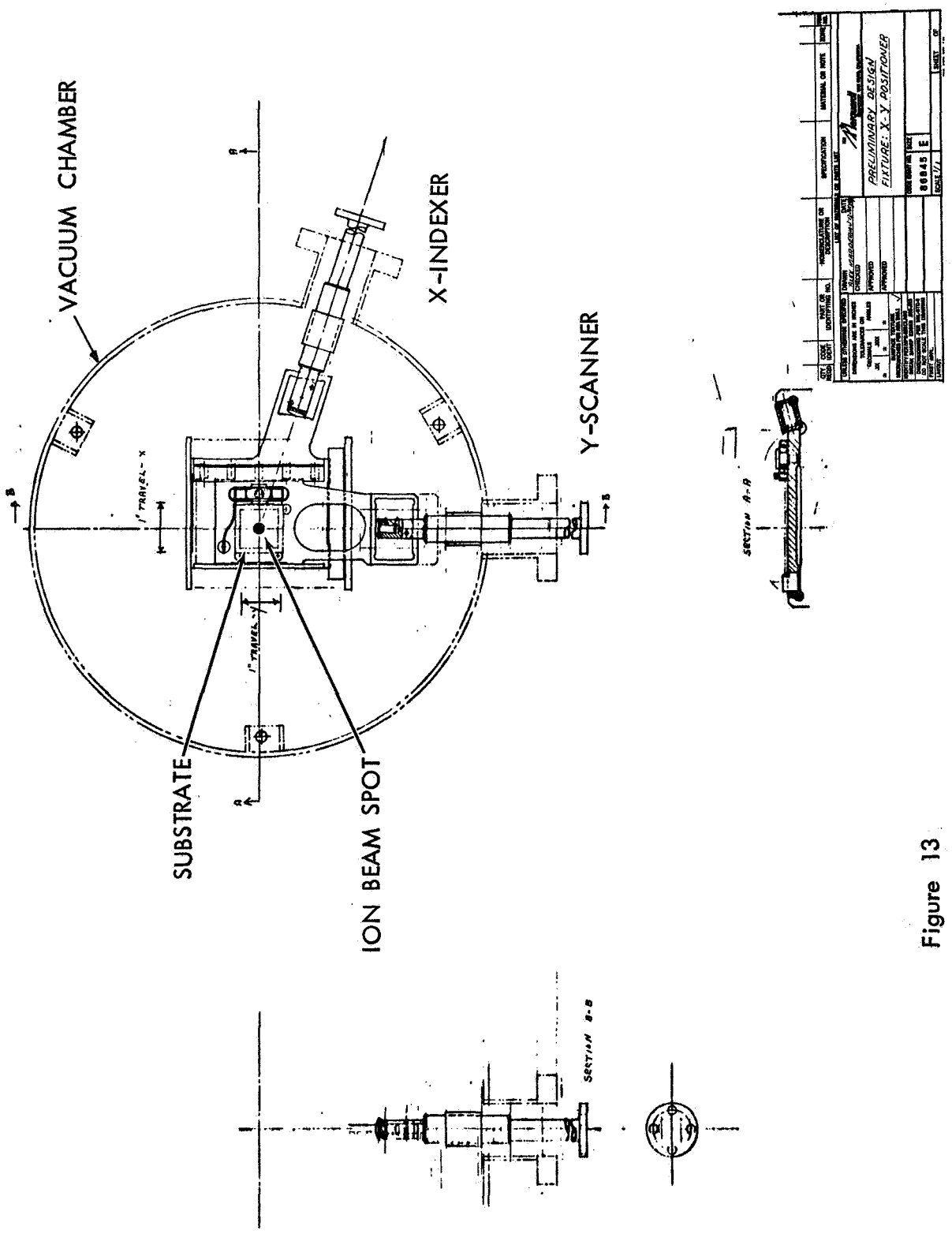


Figure 13

PRELIMINARY DESIGN FIXTURE; X-Y POSITIONER

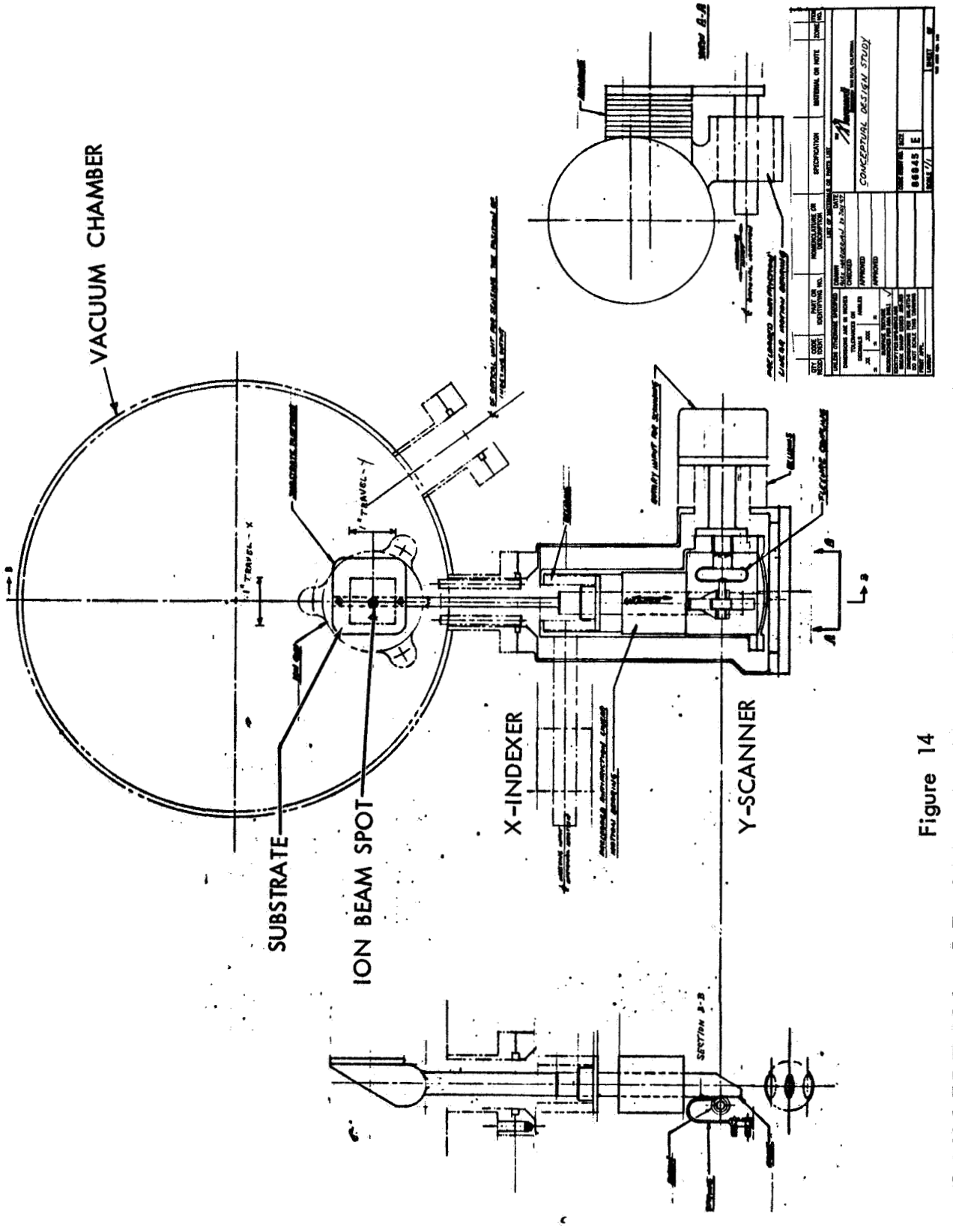


Figure 14

CONCEPTUAL DESIGN STUDY; X-Y POSITIONER

for moving the substrate over a distance of 1 inch with an accuracy of 0.1 mil. This capability is sufficient to investigate the ion beam scan speed required in the implantation process.

BREADBOARD MODEL DEVELOPMENT

A breadboard 2 axis commutator was designed and fabricated to demonstrate the line skip function. A hybrid thin film configuration was selected for this experimental implementation.

Circuits

Three basic circuits are used to implement the hybrid line skip commutators; a conventional flip-flop, an output driver, and a driver for reset. (See Figures 15, 16 and 17). The binary storage unit (BS) is a flip-flop with provision for binary reset and emitter follower amplifiers to provide for a buffered output. The readout driver (RD) consists of a negative AND gate followed by several buffer amplifiers. A positive voltage on any of the diode inputs can furnish sufficient drive to saturate the following inverter amplifier. A Readout Trigger voltage pulse furnishes the collector supply for this amplifier and no output will be obtained for the above condition. However, if all diode inputs are near ground level, application of the Readout Trigger will cause the following stages to be driven into saturation thus providing a DC output from the readout driver. This same pulse will be differentiated by the binary reset diode network and is available for application to the flip-flops mentioned above. The reset line driver (RLD) uses two inverting amplifiers to furnish a normalized voltage pulse for initial resetting purposes. In addition to the above, a small diode network is used for output decoding purposes. Figure 18 indicates in block form the interconnection of the various circuits.

A breadboard of this circuit was first constructed with conventional components to verify correct performance and to serve as test instrumentation for testing ferroelectric elements. This breadboard is shown in Figure 19.

Construction

The breadboard model consists of, besides the 2 axis line skip commutator, a simulated 5 x 5 image plate matrix, and the necessary control circuitries.

In order to implement the commutator in hybrid thin film form, two layouts representing the patterns for the resistive elements, land areas for the semiconductors, and the conductors are made with a precision coordinatograph. From this artwork the various masks are prepared by a photoetching process. Resistors and conductors are then vacuum deposited. Discrete microcircuit components are connected by eutectic bonding techniques. As a final operation, one mil wire is bonded to complete the interface connection between the substrate and the package terminal posts. The required hybrid circuits for the

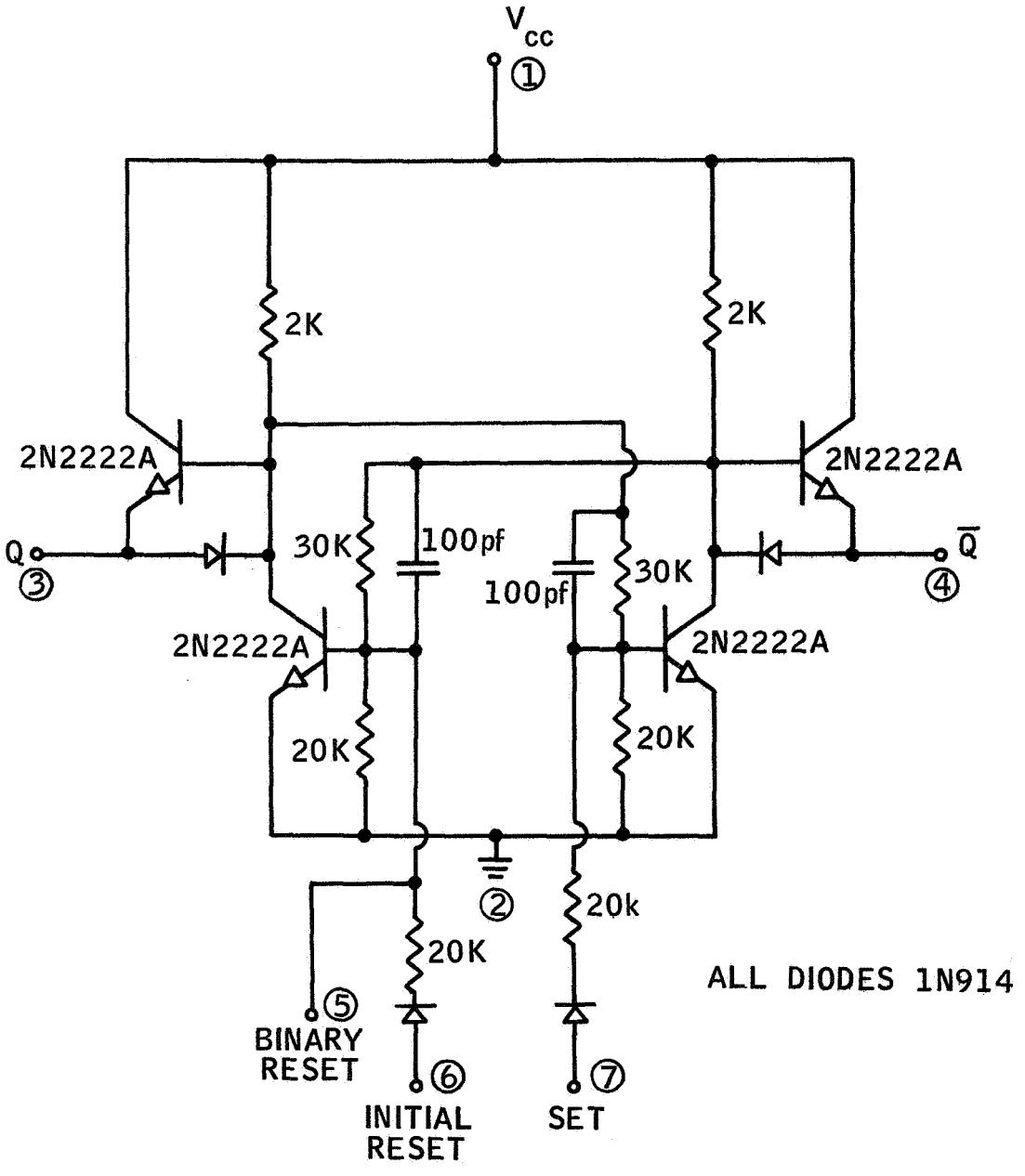


Figure 15

BINARY STORAGE UNIT (BS)

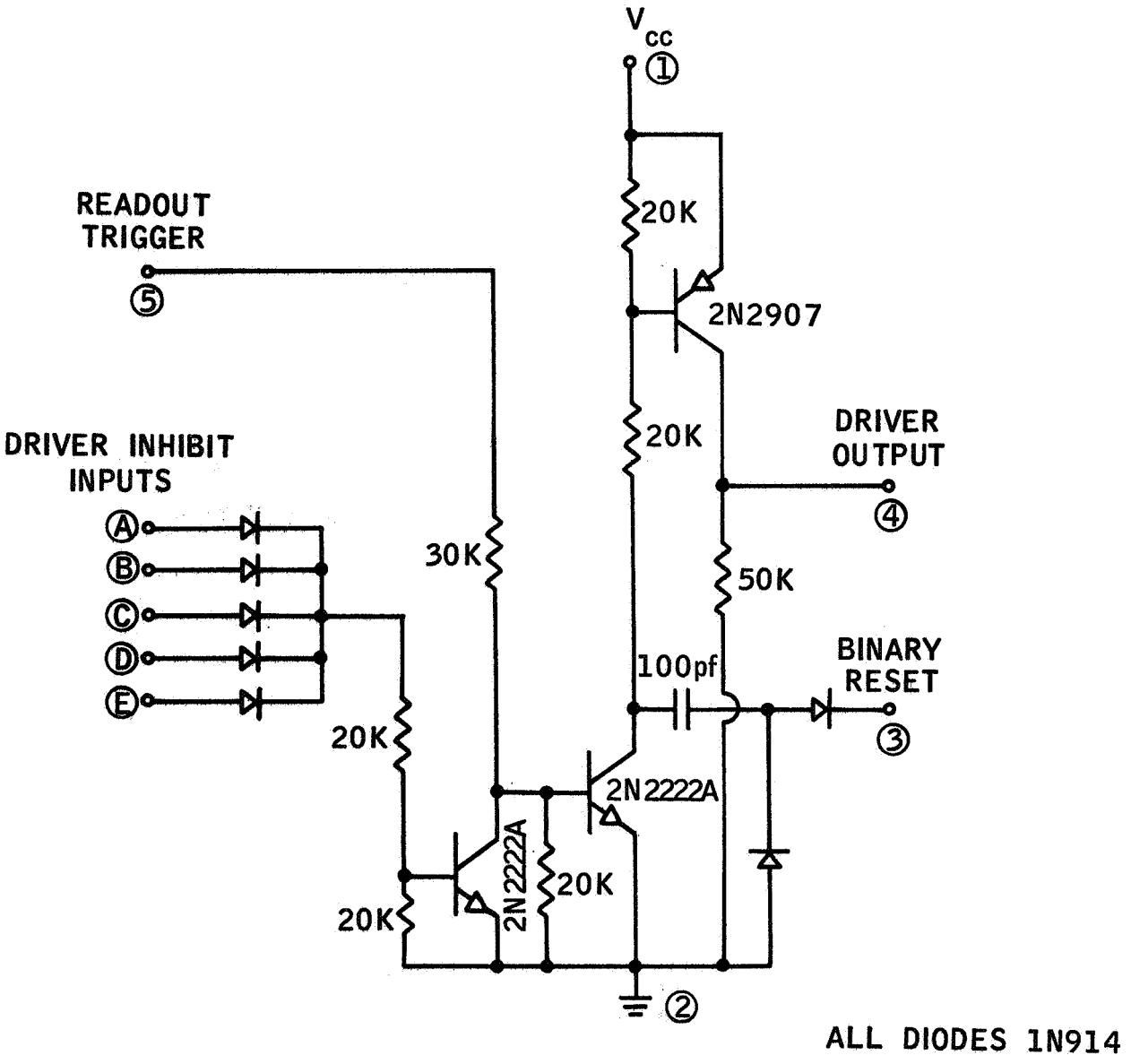


Figure 16

READOUT DRIVER (RD)

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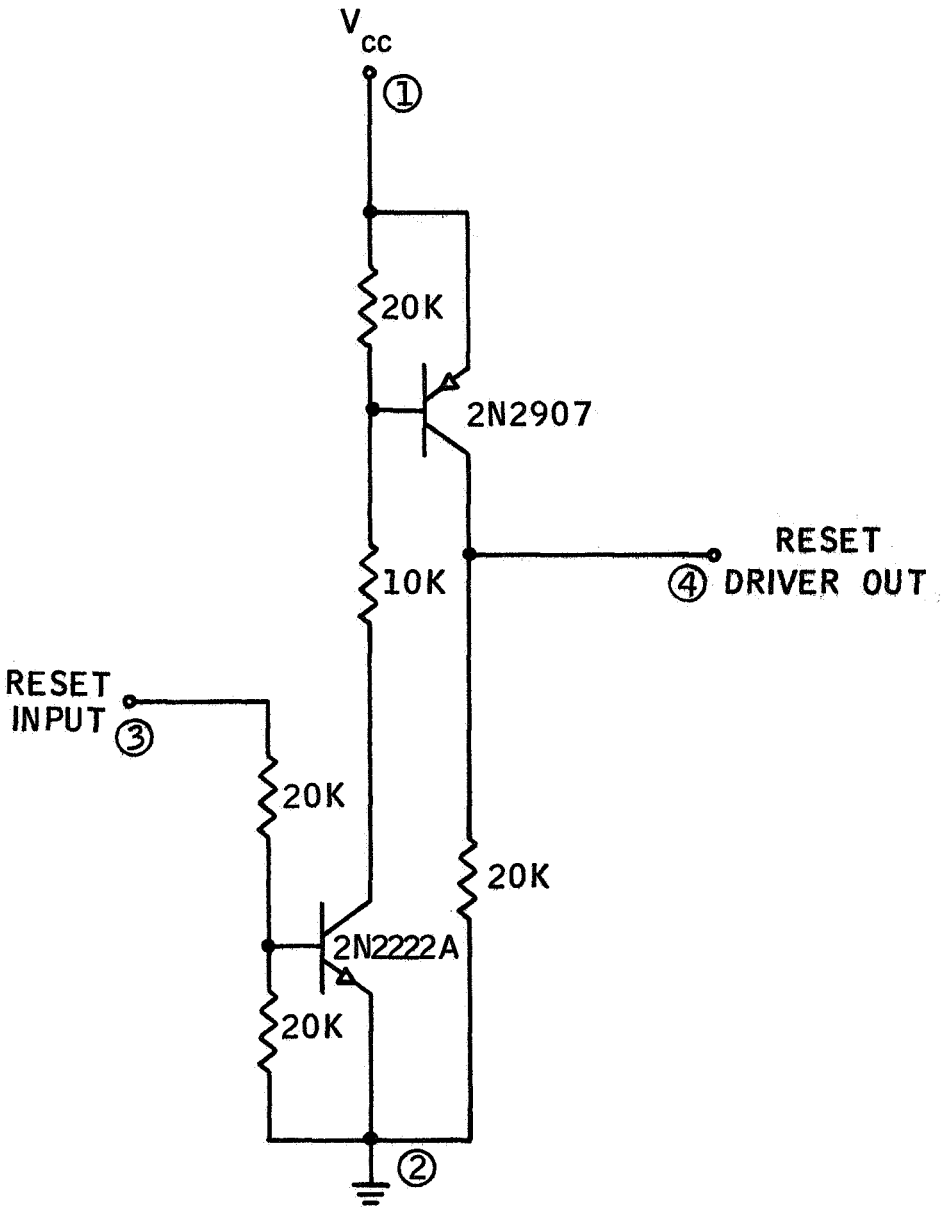


Figure 17

RESET LINE DRIVER (RLD)

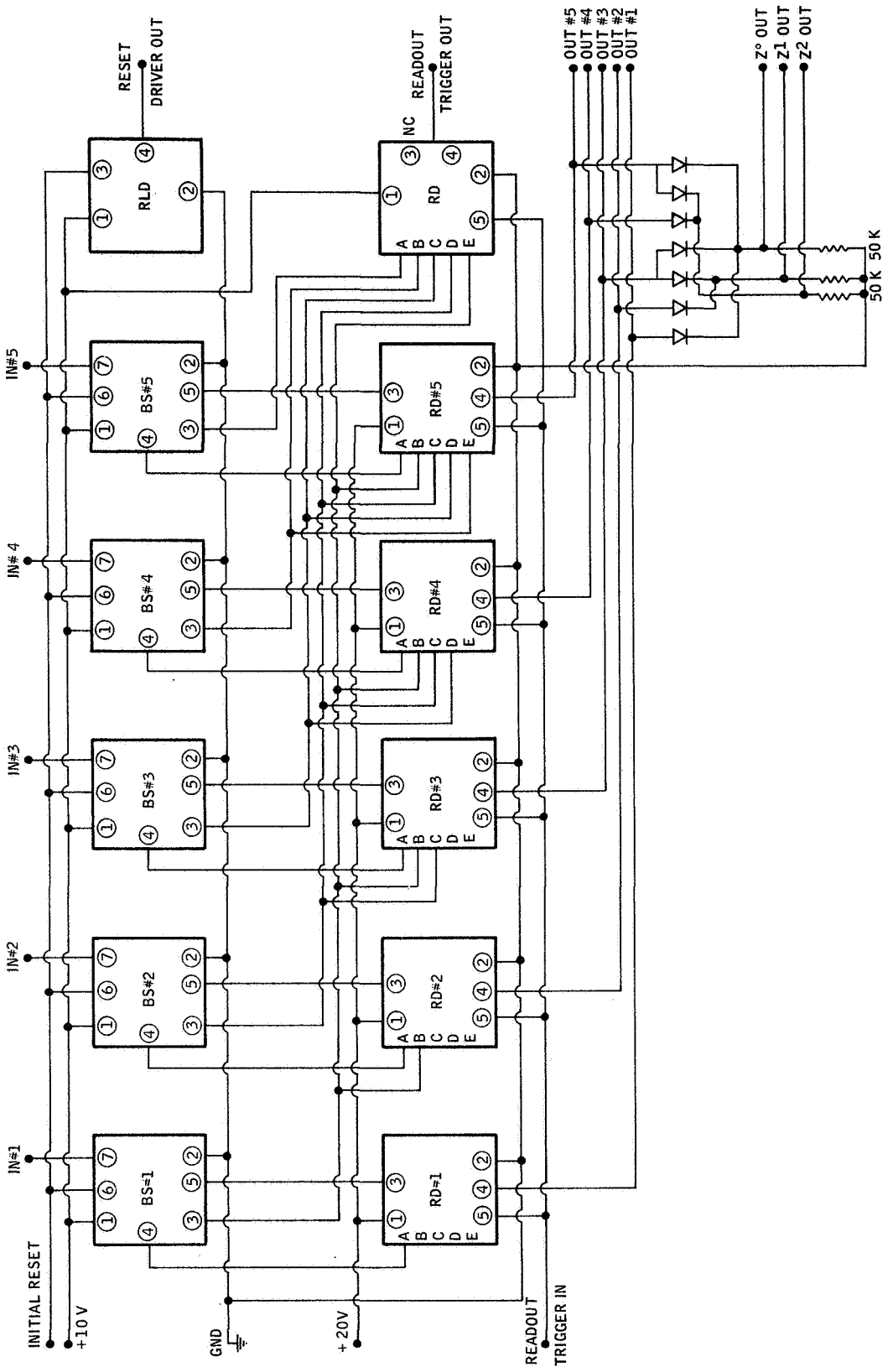


Figure 18

INTERCONNECTION OF COMMUTATOR LOGIC

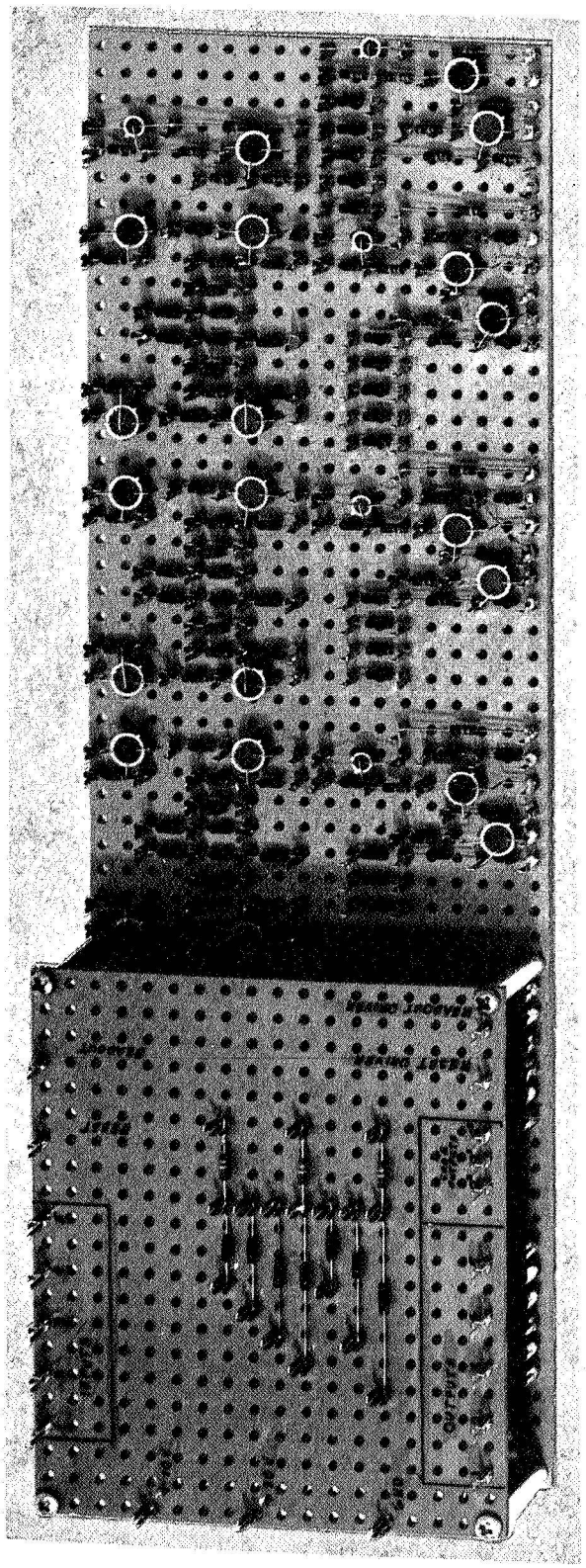


Figure 19
HYBRID BREADBOARD TEST CIRCUIT

row and column axis are housed in two flat packs each with 1 x 1 inch dimensions. Figure 20 depicts the inside of such a flat pack.

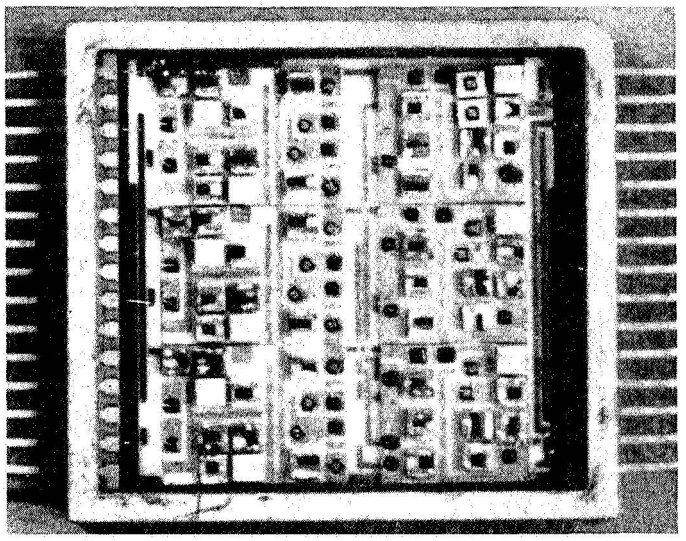
The simulated image sensor matrix consists of twenty-five ferroelectric elements housed in conventional transistor cases. The elements were fabricated from a lead titanate zirconate ferroelectric material. This ferroelectric exhibits a spontaneous polarization of approximately 30 microcoulombs per square centimeter and a coercive field of approximately 6000-8000 volts per centimeter. A one mil slab of the material was electroded with 35 square mil dots and ultrasonically machined to produce elemental areas. The ferroelectric elements simulate the storage portion of a photoconductive-ferroelectric laminate. In such a laminate (see Appendix A) the incident light would allow the photoconductors to pass current which, in turn, would be stored in the associated ferroelectric elements. In this model conventional switches are used to simulate the photoconductor gating function instead of the laminate to provide flexibility in testing.

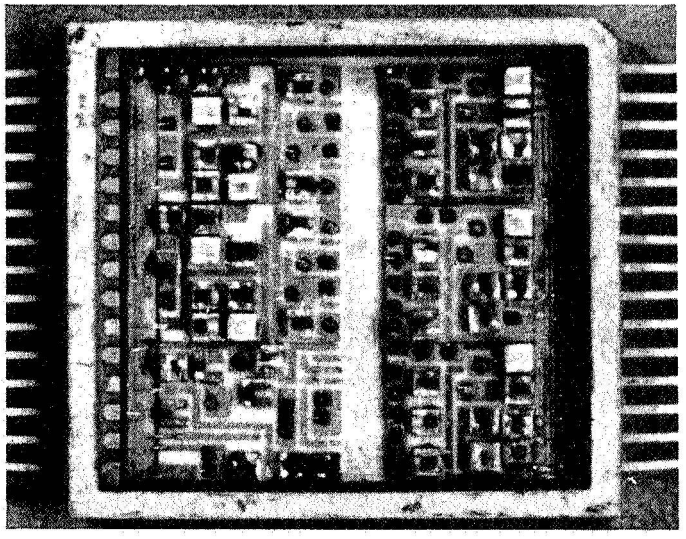
The 4 flat packs and the 25 element matrix are housed in a common chassis together with the various switches and terminals necessary to control and observe the operating sequence. Figure 21 indicates the interconnections of these components and Figure 22 shows a picture of the entire breadboard model.

Evaluation

To prepare the hybrid breadboard for operation it is necessary to ascertain that all of the ferroelectric elements have a like polarity. To perform this operation, each element is inserted into the FE POLARIZE socket provided on the chassis (a colored dot distinguishes between the two terminals of the element case), the SELECT switch set to POLARIZE, and the pushbutton depressed. After polarization and reinsertion of the elements in the matrix, the SELECT switch is set to INITIAL RESET and the button depressed to insure that all stages of both line skip commutators have been cleared of digital data.

For data entry into the desired ferroelectric elements, the pertinent ROW SELECT and COLUMN SELECT switches are operated. The SELECT switch is set to SET TAG and the button is depressed to apply voltage to switch the selected ferroelectric elements. Their switching sets the corresponding binary storage (BS) units of the column line skip commutator. The select switches are now returned to their original position. In an operational system, these switches would be replaced by electronic gating circuits. With the SELECT switch set to COLUMN READ, a strobe pulse is applied to the read-out driver of the first binary storage unit containing data. The output from this stage is fed to the decoding network and a binary coded output identifies the appropriate column. Simultaneously, a reset pulse is furnished to the storage unit and voltage is applied to the pertinent column of the matrix thus setting the ferroelectric element to its original state of





1 in. x 1 in. ACTUAL SIZE

Figure 20

HYBRID BREADBOARD MODEL FLAT PACKS

INTERNAL VIEWS

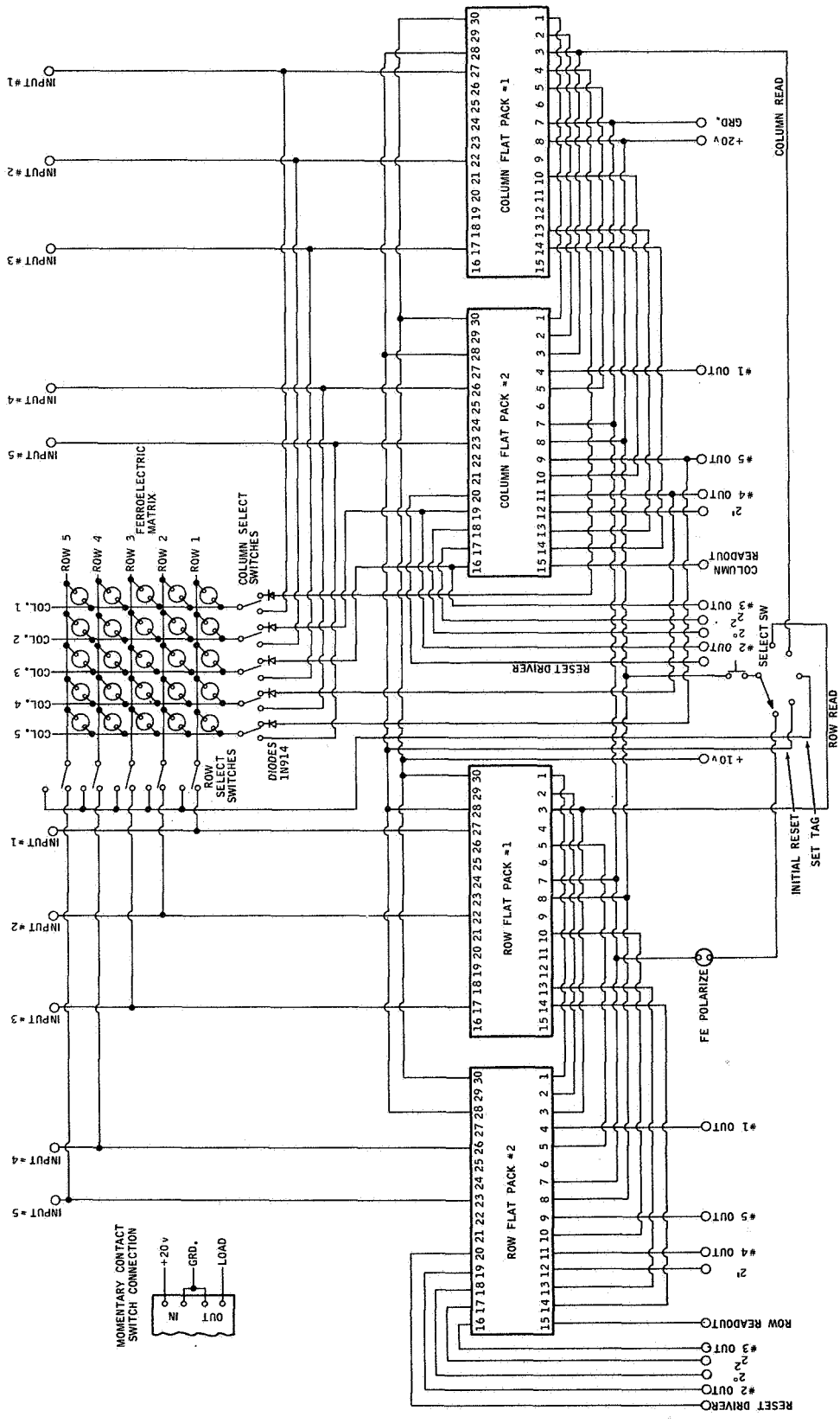


Figure 21

HYBRID BREADBOARD INTERCONNECTION

R-26,912

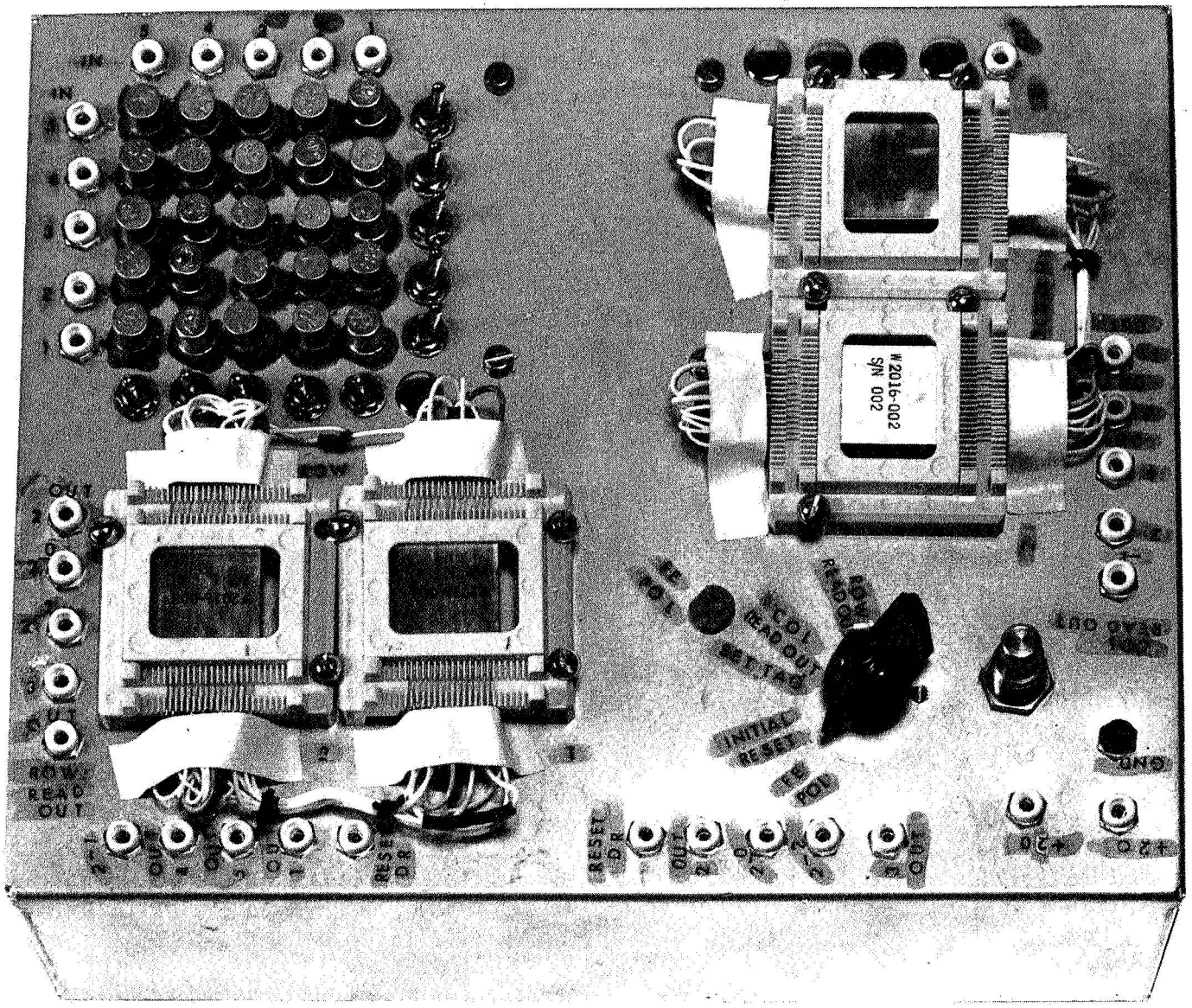


Figure 22

HYBRID BREADBOARD MODEL ASSEMBLY

R-26,913
Neg. 9457-1
44

polarization. As the element is switched, current is fed to the corresponding binary storage unit in the row line skip commutator. This operation could involve a number of ferroelectric elements (if more than one element had originally been selected in the same column) and thus a number of storage units could be tagged. With the SELECT switch in the ROW READ position, depression of the button now provides a binary coded output that identifies the correct row. This cycle is repeated by selecting the COLUMN READ and sequentially the ROW READ to read out the remaining data points in the matrix. An indication that all data has been read out is obtained when depression of the button in the COLUMN READ position does not produce an output.

Test of the hybrid breadboard consisted of following the above sequence to insure that correct outputs were obtained for various combinations of matrix points. It was verified that a non-ambiguous matrix line skip operation is feasible, i.e., the positions of diagonally placed data points were identified uniquely with their corresponding x-y binary code. However, the insufficient hysteresis loop characteristic of the lead titanate zirconate ferroelectric material used to simulate the image plate caused a considerable crosstalk between matrix data points so that the operable number of points was limited to ten.

CONCLUSIONS AND RECOMMENDATIONS

The results obtained to date in the investigation of line skip commutator techniques allow the following conclusions:

The line skip commutator is a practical mechanism for the fast readout of matrix image sensors with low data content such as required in a celestial field scanner application, as indicated by tests with a hybrid thin film breadboard implementation.

The logic functions of the line skip commutator can be implemented with integrated thin film transistor (TFT) circuitries based on analysis and evaluation of individual TFT's.

The high elemental packing density desired for the implementation of the circuits can possibly be accomplished with ion implantation techniques according to a design study.

The further development of the ion implantation technique is recommended to produce the commutator in integrated TFT circuitry configuration.

APPENDIX A

FERROTRON IMAGE TRANSDUCER CONCEPT

APPENDIX A

FERROTRON IMAGE TRANSDUCER CONCEPT

The concept of Marquardt's thin film solid state sensor/scanner plate or image transducer capable of satisfying many advanced image sensing functions is described below. The general image transducer plate configuration is shown in Figure A-1. It is a single laminate of solid state materials for performing the two functions of image transducing, i.e., the sensing/storage and the readout/commutating functions. Fine electrode lines are deposited on each side of the laminate orthogonally to each other, thereby dividing the sensor plate effectively into small elemental areas for readout purposes. Either a continuous exposure mode or a frame exposure mode of operation could be employed. In the latter case, an electric shutter pulse exposes effectively the sensing area to the projected image. The optical image is thereby transduced into a latent image in the form of a charge pattern which is retained until readout. The stored image is read out by rapidly commutating the rows and columns of the electrode matrix. Each switched matrix point produces a video signal proportional to the stored charge.

The sensing portion of the image transducer plate is composed of thin film layers of photoconductor/ferroelectric/electrode materials and a supporting glass substrate. The front electrode is transparent to allow the light from the scene to reach the photoconductor. An elemental area of the laminate and an equivalent circuit is shown in Figure A-2. The photoconductor (PC) can be thought of as a variable resistor whose conductivity is approximately proportional to the intensity of the incident light (Figure A-3). The ferroelectric (FE) can be thought of as a non-linear capacitor across which an internal polarization (charge) is accumulated as a function of the time integral of the current flow. The internal polarization of the FE follows a voltage/charge hysteresis pattern analogous to the more familiar ferromagnetic B/H hysteresis phenomena. The stored charge, i.e., internal polarization will not leak off in time as occurs with the charge in purely dielectric materials employed in conventional capacitors. As a result, there is no loss in the analog signal amplitude between exposure and read-in operations.

In operation, light impinging on an element from a radiant source will cause the photoconductor to become more conductive than in its dark state. During exposure, a voltage is applied across the element causing current, determined by the PC resistance to flow through the photoconductor and charge up the FE material. The charge value is retained until an opposite voltage is applied for readout. Since a fractional polarization is a function of the photoconductor current and time duration of the read-in pulse applied to

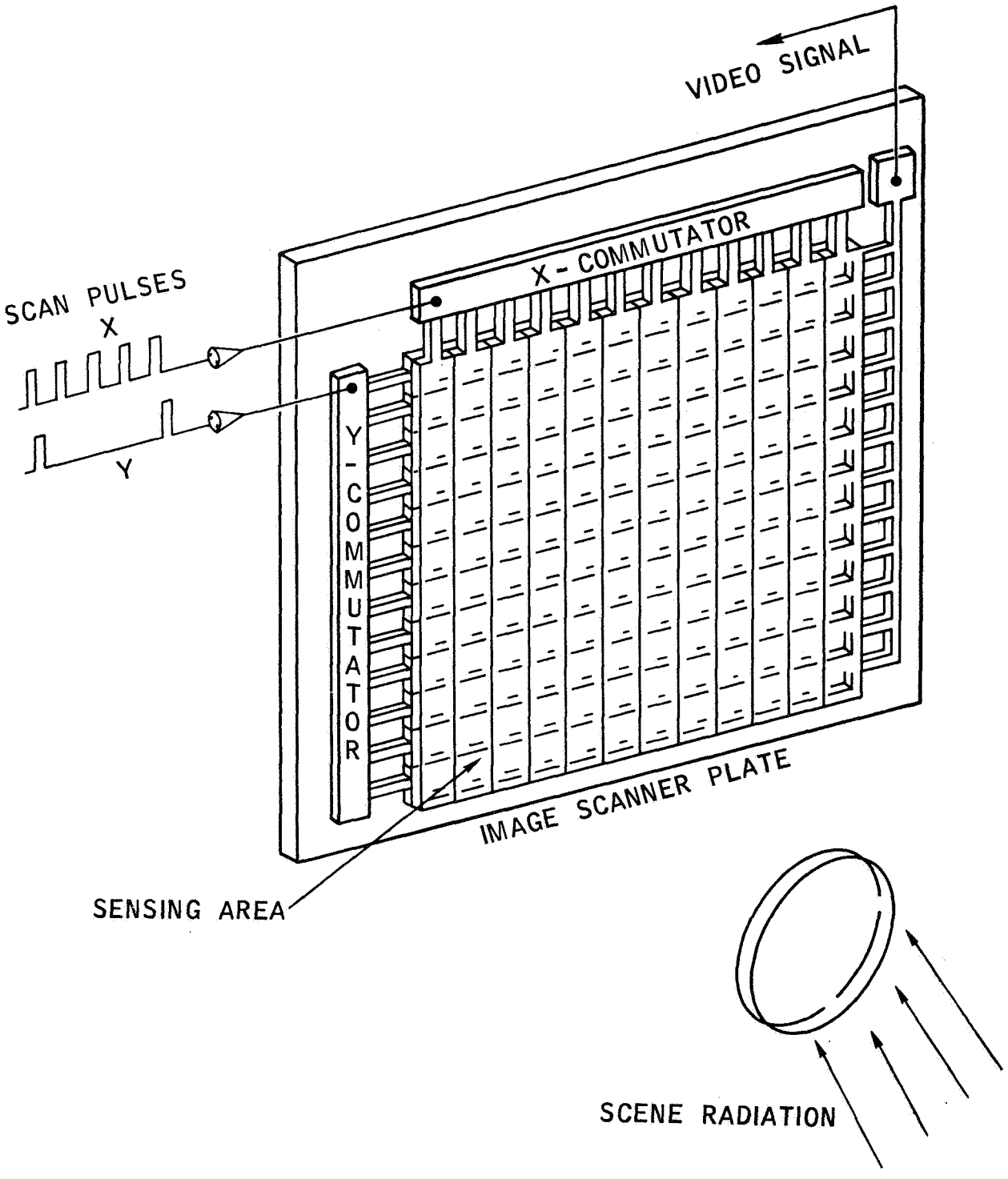
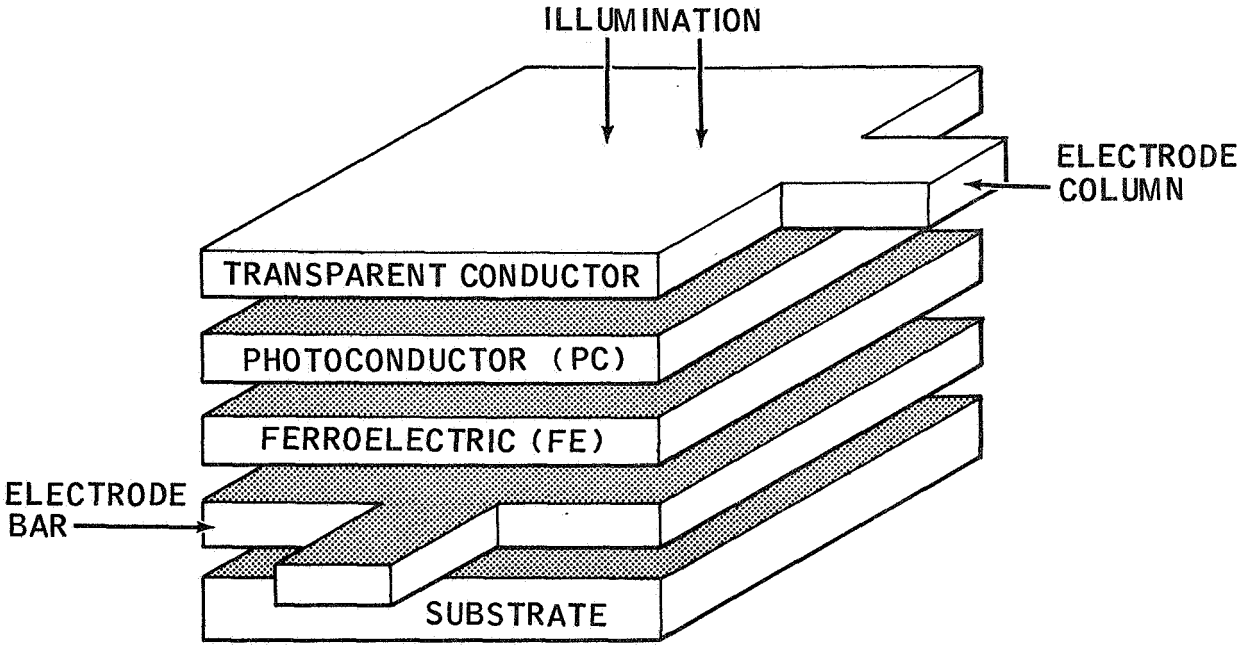
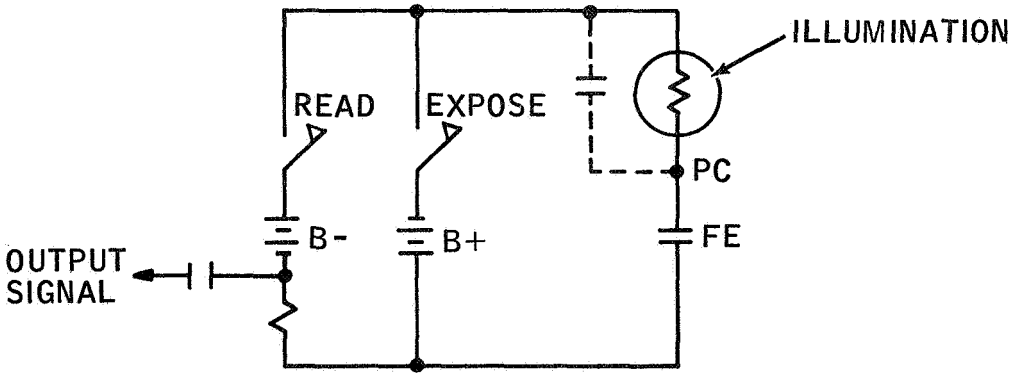


Figure A-1

IMAGE SENSOR WITH OPTO-ELECTRONIC READ OUT



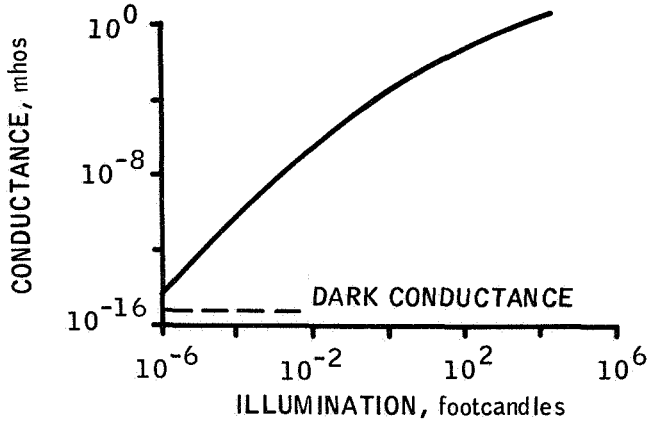
A. LAMINATE



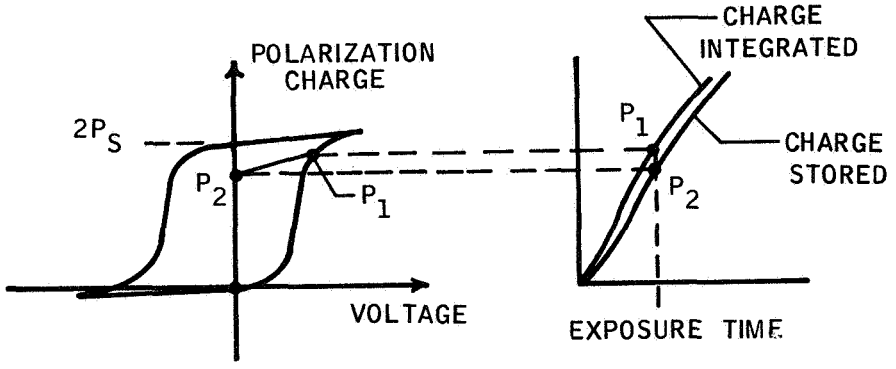
B. EQUIVALENT CIRCUIT

Figure A-2

SENSOR ELEMENT



(A) CdS PHOTO CONDUCTOR



(B) CHARGE RETENTION BY A NON-LINEAR FERROELECTRIC CAPACITOR

Figure A-3

IMAGE PLATE MATERIAL CHARACTERISTICS

it, it represents a grey scale of an image point (Figure A-4). The dynamic range and thereby the gamma of the sensor can be varied by changing the amplitude and time duration of the read-in voltage applied to it. The application of an opposite voltage to the ferroelectric element results in a current which discharges the stored data and returns the FE to its original state of polarization. To effect the ferroelectric readout it is necessary to lower the resistance of the photoconductor. For this purpose, the photoconductor is driven into its space charge limited state by the application of a high electric field which will result in the delivery of a very high current to the FE independent of illumination. (Figure A-5).

Figure A-6 shows a complete write/read cycle where the readout current time integral is proportional to the read-in current time integral, which, in turn, is representative of the light intensity at that image point. Inasmuch as the readout time is considerably shorter than the exposure time, a high current level, low impedance output signal is realized.

In the image sensor plate an elemental readout current is obtained at the intersection point of the front electrode bar and back electrode column pair that is switched on. The desired sequence of bar and column switching would depend on the particular application requirements. For example, in a conventional image transducer application a raster mode scan sequence would be employed. In this case, the electrode bars are switched on in incremental steps. At each "bar" step position all the columns are switched one after another in rapid sequence. In this manner, the latent image is dissected point by point, producing the appropriate video signals required to transduce a complete image.

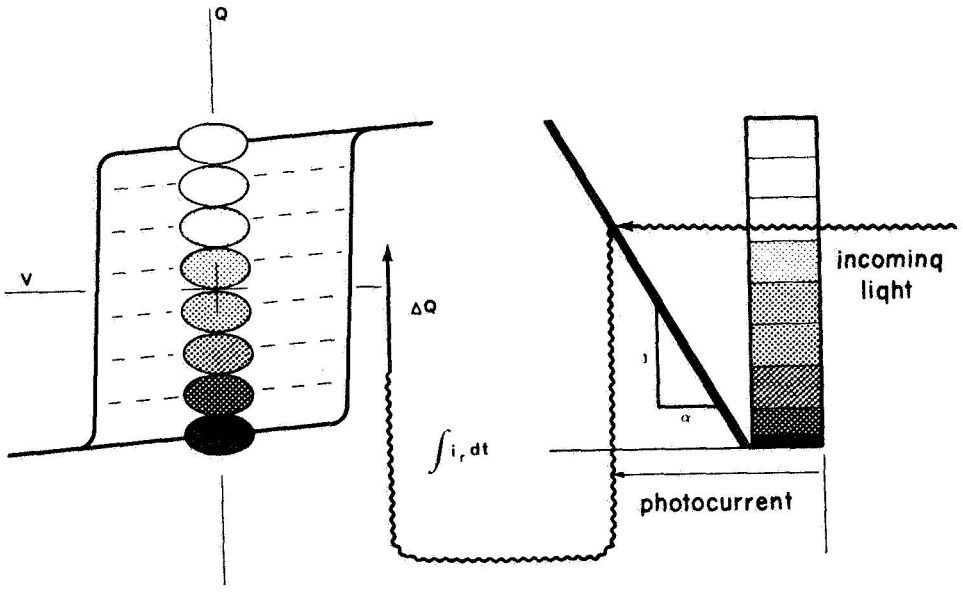
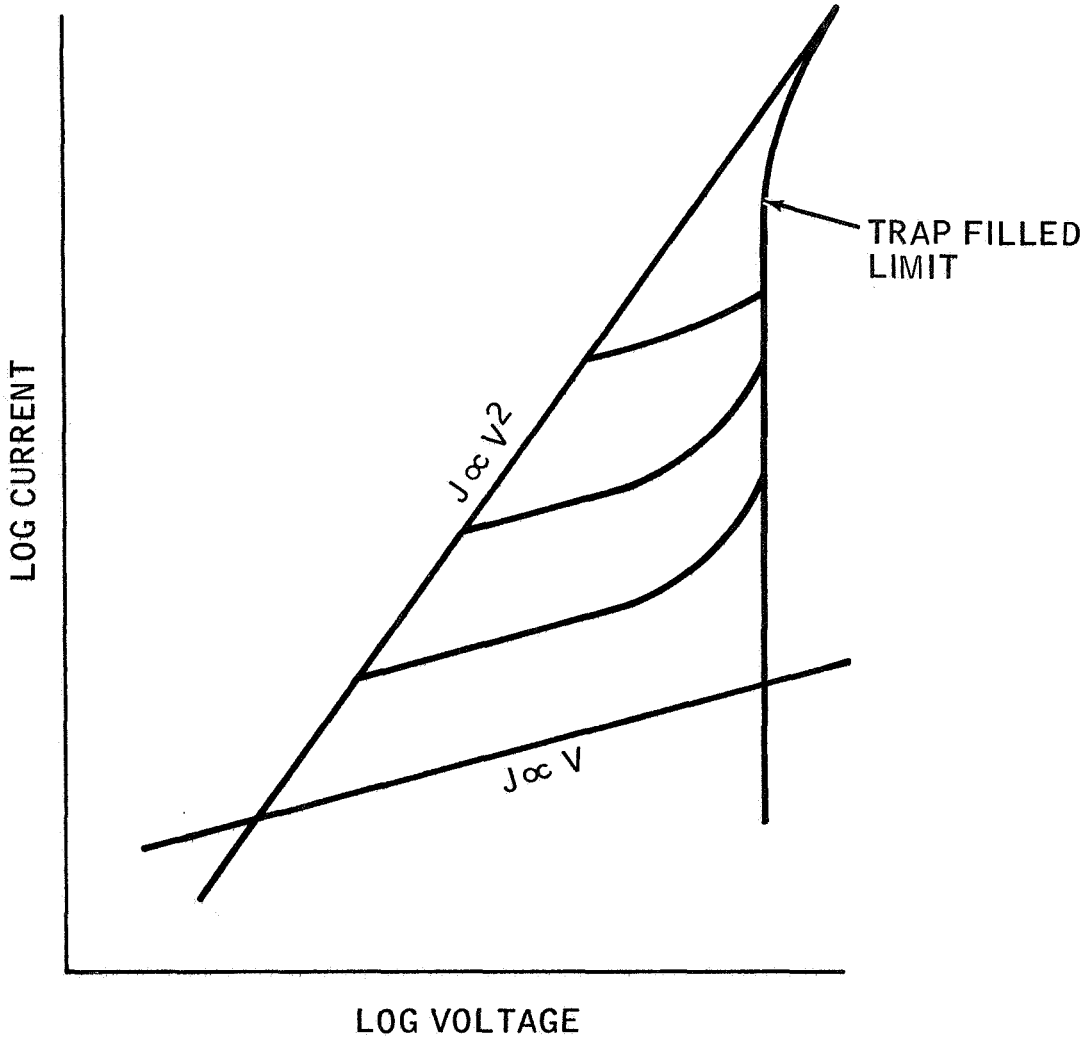


Figure A-4

RELATION OF GRAY SCALE TO POLARIZATION



AS INDICATED BY THE TRAP FILLED LIMIT LINE, THE CURRENT (AND HENCE CONDUCTIVITY) OF A PHOTOCONDUCTOR BECOMES VERY LARGE AND INDEPENDENT OF ILLUMINATION FOR SUFFICIENTLY LARGE APPLIED VOLTAGE.

Figure A-5

SPACE CHARGE LIMITATION OF A TYPICAL PHOTOCONDUCTOR